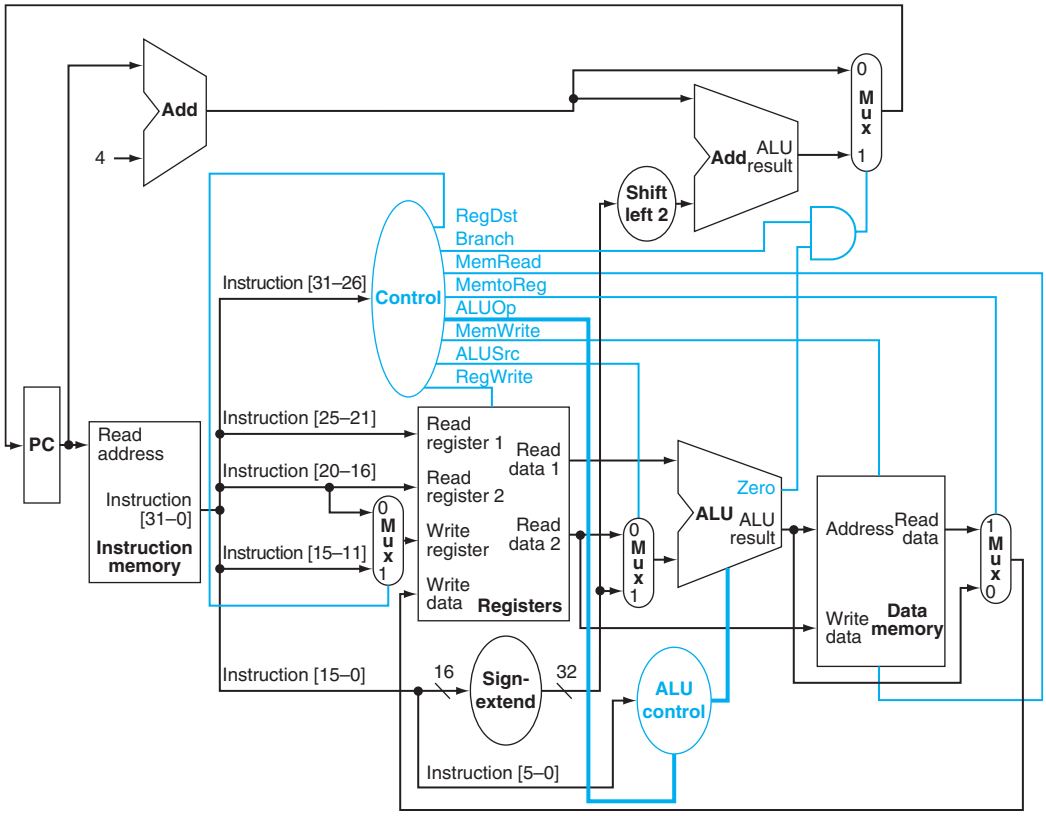
CSEE 3827: Problem Set 7 — Due: 4/27/09

Complete the following problems. Be sure to show your work for partial credit.

1. Assume `Instruction[31-0] = 00000001001001000100000000100100`. Label all of the wires in the single-cycle MIPS datapath shown below with their values at the end of the clock cycle in which the above instruction was fetched. Rather than assume particular register or PC contents, you may label the wires symbolically (e.g., as "PC" or "Reg[3]+Reg[6]").



2. Given the MIPS datapath shown above (and in Figure 4.17 of the text), assume the component latencies in the following table.

I-Mem	400ps
Add	100ps
Mux	30ps
ALU	120ps
Regs	200ps
D-Mem	350ps
Control	100ps
ALU Control	50ps
Shift Left	30ps
Sign Extend	30ps

(a) What is the critical path for a MIPS `or` instruction?

(b) What is the critical path for a MIPS `lw` instruction?

(c) What is the critical path for a MIPS `beq` instruction?

(d) What is the clock cycle time for this processor?

(e) If your colleague optimizes the adder and reduces its latency to 75ps, what is the clock cycle time of the new version?