Constraints Guide

ISE 7.1i

XILINX®

About This Guide

This chapter contains the following sections:

Guide Contents

This guide contains the following chapters:

Additional Resources

For additional information, go to: http://www.xilinx.com. The following table lists some of the resources you can access from this Website. You can also directly access these resources using the provided URLs.

Resource	Description
Tutorials	Tutorials covering Xilinx design flows, from design entry to verification and debugging http://www.xilinx.com/support/techsup/tutorials/index.htm
Answer Browser	Database of Xilinx solution records http://www.xilinx.com/xlnx/xil_ans_browser.jsp
Application Notes	Descriptions of device-specific design techniques and approaches http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp?category=Application+Notes
Data Sheets	Device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp

Resource	Description
Problem Solvers	Interactive tools that allow you to troubleshoot your design issues http://www.xilinx.com/support/troubleshoot/psolvers.htm
Tech Tips	Latest news, design tips, and patch information for the Xilinx design environment http://www.xilinx.com/xlnx/xil_tt_home.jsp

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	**`ngdbuild`** *`design_name`*
	References to other manuals	See the *Development System Reference Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Square brackets [ ]	An optional entry or parameter. However, in bus specifications, such as **`bus[7:0]`**, they are required.	**`ngdbuild`** [*`option_name`*] *`design_name`*
Braces { }	A list of items from which you must choose one or more	**`lowpwr ={on|off}`**
Vertical bar |	Separates items in a list of choices	**`lowpwr ={on|off}`**

Convention	Meaning or Use	Example

Vertical ellipsis
.
.
.
	Repetitive material that has been omitted	`IOB #1: Name = QOUT'`
		`IOB #2: Name = CLKIN'`
		.
		.
		.

Horizontal ellipsis ...	Repetitive material that has been omitted	**`allow block`** *block_name loc1 loc2 ... locn;*

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current file or in another file in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the *Virtex-II Handbook*.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

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Chapter 4: Timing Constraint Strategies

Chapter 5: Third-Party Constraints

Chapter 6: Alphabetized List of Xilinx Constraints

Chapter 1

Introduction

This chapter presents an overview of Xilinx constraints, according the following features:

- Each constraint, constraint type, and the architectures associated with each constraint.
- Each constraint and the entry strategy associated with it.

Constraint Type and Supported Architectures

The following table lists constraint types and architectures, as follows:

- The Constraint Type column shows the general category for the constraint, timing, placement, grouping, mapping, routing, modular design, synthesis, fitter, initialization, and DLL/DCM.
- The Architectures columns show which Xilinx devices are supported for each constraint. Only architectures dating from Spartan-3 are included in this table. Contact Xilinx Customer Support if information is needed for older Xilinx architectures.

Table 1-1: **Constraints, Types, and Supported Architectures**

Click the name of the constraint for which you want more detailed information.

Constraint	Constraint Type										Architectures						
	Timing	Placement	Grouping	Mapping	Routing	Modular Design	Synthesis	Fitter	Initialization	DLL/DCM	Spartan-3	Virtex-II	Virtex-II Pro/X	Virtex-4	XC9500 families	CoolRunnerXPLA3	CoolRunner-II
AREA_GROUP		√		√	√	√					√	√	√	√			
ASYNC_REG	√										√	√	√	√			
BEL		√									√	√	√	√			
BLKNM				√							√	√	√	√			
BOX_TYPE							√				√	√	√	√	√	√	
BRAM_MAP				√							√	√	√	√			
BUFFER_TYPE							√				√	√	√	√			
BUFG (CPLD)							√	√							√	√	√

Constraint	Constraint Type										Architectures						
	Timing	Placement	Grouping	Mapping	Routing	Modular Design	Synthesis	Fitter	Initialization	DLL/DCM	Spartan-3	Virtex-II	Virtex-II Pro/X	Virtex-4	XC9500 families	CoolRunnerXPLA3	CoolRunner-II
BUFGCE							√				√	√	√	√			
CLK_FEEDBACK										√	√	√	√	√			
CLKDV_DIVIDE										√	√	√	√	√			
CLKFX_DIVIDE										√	√	√	√	√			
CLKFX_MULTIPLY										√	√	√	√	√			
CLKIN_DIVIDE_BY_2										√	√	√	√	√			
CLKIN_PERIOD										√	√	√	√	√			
CLKOUT_PHASE_SHIFT										√	√	√	√	√			
CLOCK_BUFFER							√				√	√	√	√			
CLOCK_SIGNAL							√				√	√	√	√			
COLLAPSE								√							√	√	√
COMPGRP			√			√					√	√	√	√			
CONFIG		√									√	√	√	√	√	√	√
CONFIG_MODE					√						√	√	√	√			
COOL_CLK								√									√
DATA_GATE								√									√
DCI_VALUE											√	√	√	√			
DECODER_EXTRACT							√				√	√	√	√			
DESKEW_ADJUST				√										√			
DFS_FREQUENCY_MODE										√	√	√	√	√			
Directed Routing					√						√	√	√	√			
DISABLE	√										√	√	√	√			
DLL_FREQUENCY_MODE										√	√	√	√	√			
DRIVE				√							√	√	√	√			
DROP_SPEC	√										√	√	√	√	√	√	√
DUTY_CYCLE_CORRECTION										√	√	√	√	√			
ENABLE	√										√	√	√	√			
ENUM_ENCODING							√				√	√	√	√	√	√	√

Constraint	Constraint Type										Architectures						
	Timing	Placement	Grouping	Mapping	Routing	Modular Design	Synthesis	Fitter	Initialization	DLL/DCM	Spartan-3	Virtex-II	Virtex-II Pro/X	Virtex-4	XC9500 families	CoolRunnerXPLA3	CoolRunner-II
EQUIVALENT_REGISTER_REMOVAL							√				√	√	√	√	√	√	√
FAST				√							√	√	√	√	√	√	√
FEEDBACK											√	√	√	√			
FILE											√	√	√	√	√	√	√
FLOAT				√											√	√	√
FROM-THRU-TO	√										√	√	√	√			
FROM-TO	√										√	√	√	√	√	√	√
FSM_ENCODING							√				√	√	√	√	√	√	√
FSM_EXTRACT							√				√	√	√	√	√	√	√
FSM_STYLE							√				√	√	√	√	√	√	√
FULL_CASE							√				√	√	√	√	√	√	√
HBLKNM				√							√	√	√	√	√	√	√
HIGH_FREQUENCY										√	√	√	√	√			
HU_SET				√							√	√	√	√			
INCREMENTAL_SYNTHESIS							√				√	√	√	√			
INIT									√		√	√	√	√	√	√	√
INIT_A									√		√	√	√				
INIT_B									√		√	√	√				
INIT_xx									√		√	√	√				
INITP_xx									√		√	√	√				
INREG								√								√	√
IOB				√			√				√	√	√	√			
IOBDELAY				√							√	√	√	√			
IOSTANDARD				√			√				√	√	√	√	√	√	√
KEEP				√			√				√	√	√	√	√	√	√
KEEP_HIERARCHY							√				√	√	√	√	√	√	√
KEEPER				√							√	√	√	√			√
LOC		√					√				√	√	√	√	√	√	√

Constraint	Constraint Type										Architectures						
	Timing	Placement	Grouping	Mapping	Routing	Modular Design	Synthesis	Fitter	Initialization	DLL/DCM	Spartan-3	Virtex-II	Virtex-II Pro/X	Virtex-4	XC9500 families	CoolRunnerXPLA3	CoolRunner-II
LOCATE		√				√					√	√	√	√			
LOCK					√						√	√	√	√			
LOCK_PINS					√						√	√	√	√			
LUT_MAP							√				√	√	√	√			
MAP				√							√	√	√	√			
MAX_FANOUT							√				√	√	√	√			
MAXDELAY	√										√	√	√	√			
MAXPT								√							√	√	√
MAXSKEW	√										√	√	√	√			
MOVE_FIRST_STAGE							√				√	√	√	√			
MOVE_LAST_STAGE							√				√	√	√	√			
MULT_STYLE							√				√	√	√	√			
MUX_EXTRACT							√				√	√	√	√	√	√	√
MUX_STYLE							√				√	√	√	√			
NODELAY				√							√	√	√	√			
NOREDUCE							√	√							√	√	√
OFFSET	√										√	√	√	√	√	√	√
ONESHOT	√										√	√	√	√			
OPEN_DRAIN								√									√
OPT_EFFORT		√			√						√	√	√	√			
OPT_LEVEL							√				√	√	√	√	√	√	√
OPT_MODE							√				√	√	√	√	√	√	√
OPTIMIZE				√							√	√	√	√			
OPTIMIZE_PRIMITIVES							√				√	√	√	√			
PARALLEL_CASE							√				√	√	√	√	√	√	√
PERIOD	√						√				√	√	√	√	√	√	√
PHASE_SHIFT										√	√	√	√	√			
PIN			√			√					√	√	√	√			

Constraint	Constraint Type										Architectures						
	Timing	Placement	Grouping	Mapping	Routing	Modular Design	Synthesis	Fitter	Initialization	DLL/DCM	Spartan-3	Virtex-II	Virtex-II Pro/X	Virtex-4	XC9500 families	CoolRunnerXPLA3	CoolRunner-II
PRIORITY	√										√	√	√	√	√	√	√
PRIORITY_EXTRACT							√				√	√	√	√			
PROHIBIT		√				√					√	√	√	√	√	√	√
PULLDOWN				√							√	√	√	√			
PULLUP				√							√	√	√	√		√	√
PWR_MODE								√							√		
RAM_EXTRACT							√				√	√	√	√			
RAM_STYLE							√				√	√	√	√			
REG								√							√	√	√
REGISTER_BALANCING							√				√	√	√	√			
REGISTER_DUPLICATION							√				√	√	√	√			
REGISTER_POWERUP							√								√	√	√
RESOURCE_SHARING							√				√	√	√	√	√	√	√
RESYNTHESIZE							√				√	√	√	√			
RLOC		√		√			√				√	√	√	√			
RLOC_ORIGIN		√		√							√	√	√	√			
RLOC_RANGE		√		√							√	√	√	√			
ROM_EXTRACT							√				√	√	√	√			
ROM_STYLE							√				√	√	√	√			
SAFE_IMPLEMENTATION							√				√	√	√	√			
SAFE_RECOVERY_STATE							√				√	√	√	√			
SAVE NET FLAG				√							√	√	√	√			
SCHMITT_TRIGGER								√									√
SHIFT_EXTRACT							√				√	√	√				
SHREG_EXTRACT							√				√	√	√	√			
SIGNAL_ENCODING							√				√	√	√	√			
SIM_COLLISION_CHECK														√			
SLEW				√				√			√	√	√	√	√	√	√

Constraint	Constraint Type										Architectures						
	Timing	Placement	Grouping	Mapping	Routing	Modular Design	Synthesis	Fitter	Initialization	DLL/DCM	Spartan-3	Virtex-II	Virtex-II Pro/X	Virtex-4	XC9500 families	CoolRunnerXPLA3	CoolRunner-II
SLICE_PACKING							√				√	√	√	√			
SLICE_UTILIZATION_RATIO							√				√	√	√	√			
SLICE_UTILIZATION_RATIO_MAXMARGIN							√				√	√	√	√			
SLOW								√							√	√	√
SRVAL									√		√	√	√	√			
SRVAL_A									√		√	√	√	√			
SRVAL_B									√		√	√	√	√			
STARTUP_WAIT										√	√	√	√	√			
SYSTEM_JITTER	√										√	√	√	√			
TEMPERATURE	√										√	√	√	√			
TIG	√						√				√	√	√	√			
TIMEGRP			√								√	√	√	√	√	√	√
TIMESPEC	√										√	√	√	√	√	√	√
TNM			√								√	√	√	√	√	√	√
TNM_NET			√								√	√	√	√			
TPSYNC			√			√					√	√	√	√			
TPTHRU			√								√	√	√	√			
TRANSLATE_OFF and TRANSLATE_ON							√				√	√	√	√	√	√	√
TRISTATE2LOGIC				√								√	√				
TSidentifier	√										√	√	√	√	√	√	√
U_SET				√							√	√	√	√			
USE_CARRY_CHAIN							√				√	√	√	√			
USE_CLOCK_ENABLE							√				√	√	√	√			
USE_DSP48							√							√			
USE_SYNC_RESET							√				√	√	√	√			
USE_SYNC_SET							√				√	√	√	√			
USE_RLOC		√		√							√	√	√	√			

Constraint	Constraint Type										Architectures						
	Timing	Placement	Grouping	Mapping	Routing	Modular Design	Synthesis	Fitter	Initialization	DLL/DCM	Spartan-3	Virtex-II	Virtex-II Pro/X	Virtex-4	XC9500 families	CoolRunnerXPLA3	CoolRunner-II
USELOWSKEWLINES					√		√										
VOLTAGE	√										√	√	√	√			
VREF								√									√
WIREAND								√							√		
WRITE_MODE				√					√		√	√	√	√			
WRITE_MODE_A				√					√		√	√	√	√			
WRITE_MODE_B				√					√		√	√	√	√			
XBLKNM				√							√	√	√	√			
XOR_COLLAPSE							√				√	√	√	√			

Constraint and Associated Entry Strategy

The following table lists the constraints and their associated entry strategies:

The Constraint Entry columns indicate the various methods for entering constraints. Entry strategies are discussed in detail in Chapter 3, "Entry Strategies for Xilinx Constraints."

Table 1-2: ***Table 1-2:*** **Entry Strategies for the Xilinx Constraints**

Click the name of the constraint for which you want more detailed information.

Constraint	Constraint Entry													
	Schematic	VHDL	Verilog	ABEL	NCF	UCF	Constraints Editor	PCF	XCF	FloorPlanner	PACE	FPGA Editor	XST Com. Line	Proj. Navigator
AREA_GROUP	√				√	√				√	√			
ASYNC_REG		√	√		√	√	√							
BEL	√	√	√		√	√								
BLKNM	√	√	√		√	√			√					
BOX_TYPE		√	√						√					
BRAM_MAP	√	√	√			√							√	
BUFFER_TYPE		√	√			√								
BUFG (CPLD)	√	√	√	√	√	√			√					
BUFGCE		√	√						√					
CLK_FEEDBACK	√	√	√		√	√								
CLKDV_DIVIDE	√	√	√		√	√			√					
CLKFX_DIVIDE	√	√	√		√	√						√		
CLKFX_MULTIPLY	√	√	√		√	√						√		
CLKIN_DIVIDE_BY_2	√	√	√			√								
CLKIN_PERIOD	√	√	√			√						√		
CLKOUT_PHASE_SHIFT	√	√	√		√	√								
CLOCK_BUFFER		√	√						√					
CLOCK_SIGNAL		√	√						√					
COLLAPSE	√	√	√		√	√								
COMPGRP								√						
CONFIG					√	√								√
CONFIG_MODE						√								
COOL_CLK	√	√	√	√	√	√								

Constraint	Constraint Entry													
	Schematic	VHDL	Verilog	ABEL	NCF	UCF	Constraints Editor	PCF	XCF	FloorPlanner	PACE	FPGA Editor	XST Com. Line	Proj. Navigator
DATA_GATE	√	√	√	√	√	√								
DCI_VALUE					√	√								
DECODER_EXTRACT		√	√											
DESKEW_ADJUST		√	√			√								
DFS_FREQUENCY_MODE	√	√	√		√	√								
DISABLE					√	√		√						
DLL_FREQUENCY_MODE	√	√	√		√	√								
DRIVE	√	√	√		√	√	√		√					
DROP_SPEC					√	√		√						
DUTY_CYCLE_CORRECTION	√	√	√		√	√			√					
ENABLE					√	√		√						
ENUM_ENCODING		√							√					
EQUIVALENT_REGISTER_REMOVAL		√	√						√				√	√
FAST	√	√	√	√	√	√	√		√					
FEEDBACK						√		√	√					
FILE	√	√	√		√	√								
FLOAT	√	√	√	√	√	√			√					
FROM-THRU-TO					√	√	√	√						
FROM-TO					√	√	√	√						
FSM_ENCODING		√	√						√				√	√
FSM_EXTRACT		√	√						√				√	√
FSM_STYLE		√	√		√	√								
FULL_CASE			√										√	√
HBLKNM	√	√	√		√	√								
HIGH_FREQUENCY	√	√	√											
HU_SET	√	√	√		√	√			√					
INCREMENTAL_SYNTHESIS		√	√						√					
INIT	√	√	√	√	√	√	√					√		

Constraint	Constraint Entry													
	Schematic	VHDL	Verilog	ABEL	NCF	UCF	Constraints Editor	PCF	XCF	FloorPlanner	PACE	FPGA Editor	XST Com. Line	Proj. Navigator
INIT_A	√	√	√		√	√								
INIT_B	√	√	√		√	√								
INIT_xx	√	√	√		√	√			√					
INITP_xx	√	√	√		√	√								
INREG	√			√		√								
IOB	√	√	√		√	√	√		√				√	√
IOBDELAY	√	√	√		√	√	√							
IOSTANDARD	√	√	√	√	√	√	√		√		√			
KEEP	√	√	√	√	√	√			√					
KEEP_HIERARCHY	√	√	√		√	√			√				√	√
KEEPER	√	√	√	√	√	√	√		√					
LOC	√	√	√	√	√	√	√	√	√	√	√			
LOCATE								√				√		
LOCK								√				√		
LOCK_PINS		√			√	√								
LUT_MAP		√	√						√					
MAP	√				√	√								
MAX_FANOUT		√	√						√				√	√
MAXDELAY														
MAXPT		√	√	√	√	√								
MAXSKEW	√	√	√		√	√		√				√		
MOVE_FIRST_STAGE		√	√						√				√	√
MOVE_LAST_STAGE		√	√						√				√	√
MULT_STYLE		√	√						√				√	√
MUX_EXTRACT		√	√						√				√	√
MUX_STYLE		√	√						√				√	√
NODELAY	√	√	√		√	√			√					
NOREDUCE	√	√	√	√	√	√			√					
OFFSET	√				√	√	√	√	√					

Constraint	Constraint Entry													
	Schematic	VHDL	Verilog	ABEL	NCF	UCF	Constraints Editor	PCF	XCF	FloorPlanner	PACE	FPGA Editor	XST Com. Line	Proj. Navigator
ONESHOT	√	√	√											√
OPEN_DRAIN	√	√	√	√	√	√			√					
OPT_EFFORT	√				√	√								√
OPT_LEVEL		√	√						√				√	√
OPT_MODE		√	√						√				√	√
OPTIMIZE	√		√		√	√								√
OPTIMIZE_PRIMITIVES	√	√	√		√	√			√					
PARALLEL_CASE			√										√	√
PERIOD	√	√	√		√	√	√	√	√			√		
PHASE_SHIFT	√	√	√		√	√						√		
PIN						√								
PRIORITY					√	√		√						
PRIORITY_EXTRACT		√	√						√				√	√
PROHIBIT		√	√		√	√	√	√		√	√	√		
PULLDOWN	√	√	√		√	√	√		√					
PULLUP	√	√	√	√	√	√	√		√					
PWR_MODE	√	√	√	√	√	√			√					
RAM_EXTRACT		√	√						√				√	√
RAM_STYLE		√	√						√				√	√
REG	√	√	√	√	√	√			√					
REGISTER_BALANCING		√	√						√				√	√
REGISTER_DUPLICATION		√	√						√					√
REGISTER_POWERUP		√							√				√	
RESOURCE_SHARING		√	√						√				√	√
RESYNTHESIZE		√	√						√					
RLOC	√	√	√		√	√			√	√				
RLOC_ORIGIN	√	√	√		√	√		√		√				
RLOC_RANGE	√	√	√		√	√		√	√					
ROM_EXTRACT		√	√						√				√	√

Constraint	Constraint Entry													
	Schematic	VHDL	Verilog	ABEL	NCF	UCF	Constraints Editor	PCF	XCF	FloorPlanner	PACE	FPGA Editor	XST Com. Line	Proj. Navigator
ROM_STYLE		√	√						√				√	√
SAVE NET FLAG	√	√	√		√	√			√					
SCHMITT_TRIGGER	√	√	√	√	√	√			√					
SHIFT_EXTRACT		√	√						√				√	√
SHREG_EXTRACT		√	√						√				√	√
SIGNAL_ENCODING		√	√						√				√	
SLEW	√	√	√		√	√	√		√					
SLICE_PACKING													√	√
SLICE_UTILIZATION_RATIO		√	√						√				√	√
SLICE_UTILIZATION_RATIO_MAXMARGIN		√	√						√				√	
SLOW	√	√	√	√	√	√	√		√					
SRVAL	√	√	√		√	√								
SRVAL_A	√	√	√		√	√								
SRVAL_B	√	√	√		√	√								
STARTUP_WAIT	√	√	√		√	√			√					
SYSTEM_JITTER	√	√	√		√	√			√					
TEMPERATURE					√	√	√	√						
TIG	√	√	√		√	√	√	√	√					
TIMEGRP						√	√	√	√					
TIMESPEC					√	√	√							
TNM	√			√	√	√	√							
TNM_NET	√				√	√	√							
TPSYNC	√				√	√								
TPTHRU	√				√	√	√							
TRANSLATE_OFF and TRANSLATE_ON		√	√											
TSidentifier					√	√	√	√				√		
U_SET	√	√	√		√	√			√					
USE_CARRY_CHAIN	√	√	√						√				√	

Constraint	Constraint Entry													
	Schematic	VHDL	Verilog	ABEL	NCF	UCF	Constraints Editor	PCF	XCF	FloorPlanner	PACE	FPGA Editor	XST Com. Line	Proj. Navigator
USE_RLOC	√	√	√		√	√			√					
USELOWSKEWLINES	√	√	√		√	√	√	√	√					
VOLTAGE					√	√	√	√						
VREF	√				√	√								
WIREAND	√	√	√		√	√								
WRITE_MODE	√	√	√		√	√								
WRITE_MODE_A	√	√	√		√	√								
WRITE_MODE_B	√	√	√		√	√								
XBLKNM	√	√	√		√	√			√					
XOR_COLLAPSE		√	√						√				√	√

Chapter 2

Constraint Types

The following sections describe constraint types:

Attributes

Constraints use hardware description language (HDL) and on schematics are sometimes called attributes. Attributes are instructions placed on symbols or nets in an FPGA or CPLD schematic to show their placement, implementation, naming, directionality, and other characteristics. This information is used by the design implementation software during placement and routing of a design.

In this manual, the terms “constraints” and “attributes” are used interchangeably.

Attributes applicable only to a certain schematic entry tool are described in the documentation for that tool. For third-party interfaces, consult Chapter 5, “Third-Party Constraints” for information on which attributes are available. Consult the third-party user interface guides for details on how these constraints are used.

See the discussion of “ Schematic Designs” in the discussion of each applicable constraint for guidelines on placing attributes on symbols on a schematic.

CPLD Fitter

Fitter constraints apply to CPLDs.

Following is a linked list of constraints that apply to CPLDs.

BUFG (CPLD)
COLLAPSE
COOL_CLK
DATA_GATE
FAST
INIT
INREG
IOSTANDARD
KEEP
KEEPER
LOC
MAXPT
NOREDUCE
OPEN_DRAIN
OFFSET
PERIOD
PROHIBIT
PULLUP
PWR_MODE
REG
SCHMITT_TRIGGER
SLOW
TIMEGRP
TIMESPEC
TNM
TSidentifier
VREF
WIREAND

DLL/DCM Constraints

These constraints apply only to Delayed Lock Loops (DLL) and Digital Clock Managers (DCM).

Following is a linked list of DLL / DCM constraints.

CLK_FEEDBACK
CLKDV_DIVIDE
CLKFX_DIVIDE
CLKFX_MULTIPLY
CLKIN_DIVIDE_BY_2
CLKIN_PERIOD
CLKOUT_PHASE_SHIFT
DESKEW_ADJUST
DFS_FREQUENCY_MODE
DLL_FREQUENCY_MODE
DUTY_CYCLE_CORRECTION
FAST
HIGH_FREQUENCY
PHASE_SHIFT
STARTUP_WAIT

Grouping Constraints

In a TS TIMESPEC attribute, you specify the set of paths to be analyzed by grouping start and end points in one of the following ways.

- Refer to a predefined group by specifying one of the corresponding keywords — FFS, PADS, LATCHES, RAMS, DSPS, BRAMS_PORTA, or BRAMS_PORTB.
- Create your own groups within a predefined group by tagging symbols with TNM (pronounced tee-name) and TNM_NET attributes. See TNM and TNM_NET.
- Create groups that are combinations of existing groups using TIMEGRP symbols. See TIMEGRP.
- Create groups by pattern matching on net names. See "Creating Groups by Pattern Matching".

Using Predefined Groups

Using predefined groups, you can refer to a group of flip-flops, input latches, pads, or RAMs by using the corresponding keywords

The following table lists the predefined groups:.

Keyword	Description
CPUS	PPC405 in Virtex-II Pro and Virtex-II Pro
FFS	- All CLB and IOB edge-triggered flip-flops - Shift Register LUTs in Virtex and derived - Dual-data-rate registers in Virtex2 and derived (includes both flip-flops in the DDR)
HSIOS	GT and GT10 in Virtex-II Pro and Virtex-II Pro X
LATCHES	All CLB and IOB level-sensitive latches
MULTS	Multipliers, both sync and async, in Virtex-II and derived
PADS	All I/O pads (typically inferred from top level HDL ports)
RAMS	- All CLB LUT RAMs, both single- and dual-port (includes both ports of dual-port) - All block RAMs, both single-and dual-port (includes both ports of dual-port)
BRAMS_PORTA	Port A of all dual-port block RAMs
BRAMS_PORTB	Port B of all dual-port block RAMs

From-To statements enable you to define timing specifications for paths between predefined groups. The following examples are TS attributes that are entered in the UCF. This method enables you to easily define default timing specifications for the design, as illustrated by the following examples.

Predefined Group Examples

UCF syntax:

```
TIMESPEC “TS01”=FROM FFS TO FFS 30;
TIMESPEC “TS02”=FROM LATCHES TO LATCHES 25;
TIMESPEC “TS03”=FROM PADS TO RAMS 70;
TIMESPEC “TS04”=FROM FFS TO PADS 55;
TIMESPEC “TS01” = FROM BRAMS_PORTA TO BRAMS_PORTB(gork*);
```

Note: For BRAMS_PORTA and BRAM_PORTB, the specification TS01 controls paths that begin at any A port and end at a B port, which drives a signal matching the pattern gork*.

BRAMS_PORTA and BRAMS_PORTB Examples

Following are some more examples of BRAMS_PORTA and BRAMS_PORTB:

```
NET "X" TNM_NET = BRAMS_PORTA groupA;
```

The TNM group groupA contains all A ports that are driven by net X. If net X is traced forward into any B port inputs, any single-port block RAM elements, or any Select RAM elements, these do not become members of groupA.

```
NET "X" TNM_NET = BRAMS_PORTB( dob* ) groupB;
```

The TNM group groupB contains each B port driven by net X, if at least one output on that B port drives a signal matching the pattern dob*.

```
INST "Y" TNM = BRAMS_PORTB groupC;
```

The TNM group groupC contains all B ports found under instance Y. If instance Y is itself a dual-port block RAM primitive, then groupC contains the B port of that instance.

```
INST "Y" TNM = BRAMS_PORTA( doa* ) groupD;
```

The TNM group groupD contains each A port found under instance Y, if at least one output on that A port drives a signal matching the pattern doa*.

```
TIMEGRP “groupE” = BRAMS_PORTA;
```

The user group groupE contains the A ports of all dual-port block RAM elements in the design. Note that this is equivalent to BRAMS_PORTA(*).

```
TIMEGRP “groupF” = BRAMS_PORTB( mem/dob* );
```

The user group groupF contains all B ports in the design, which drives a signal matching the pattern mem / dob*.

A predefined group can also carry a name qualifier; the qualifier can appear any place where the predefined group is used. This name qualifier restricts the number of elements being referred to. The syntax used is as follows:

```
predefined group (name_qualifier [ name_qualifier ])
```

name_qualifier is the full hierarchical name of the net that is sourced by the primitive being identified.

The name qualifier can include wildcard characters (*) to show any number of characters (or ? to show a single character), which allows the specification of more than one net or allows you to shorten the full hierarchical name to something that is easier to type.

As an example, specifying the group FFS(MACRO_A / Q?) selects only the flip-flops driving the Q0, Q1, Q2 and Q3 nets.

Following is a list of the grouping constraints:

- COMPGRP
- PIN
- TIMEGRP
- TNM
- TNM_NET
- TPSYNC
- TPTHRU

Initialization Directives

These directives initialize or configure various states for components. For example, INIT initializes ROMs, RAMs, registers, and look-up tables.

Following is a list of initialization directives.

- INIT
- INIT_A
- INIT_B
- INIT_xx
- INITP_xx
- SRVAL
- SRVAL_A
- SRVAL_B
- WRITE_MODE
- WRITE_MODE_A
- WRITE_MODE_B

Logical and Physical Constraints

The following sections explain logical and physical constraints.

Logical Constraints

Logical constraints are constraints that are attached to elements in the design prior to mapping or fitting. Applying logical constraints helps you to adapt your design's performance to expected worst-case conditions. Later, when you choose a specific Xilinx architecture and place and route or fit your design, the logical constraints are converted into physical constraints.

You can attach logical constraints using attributes in the input design, which are written into the Netlist Constraints File (NCF), or with a User Constraints File (UCF).

Three categories of logical constraints are:

- Placement Constraints
- Relative Location (RLOC) Constraints
- Timing Constraints

For FPGAs, relative location constraints (RLOCs) group logic elements into discrete sets and allow you to define the location of any element within the set relative to other elements in the set, regardless of eventual placement in the overall design. See "Relative Location (RLOC) Constraints" for more information on RLOCs.

Timing constraints allow you to specify the maximum allowable delay or skew on any given set of paths or nets in your design.

Physical Constraints

Constraints can also be attached to the elements in the physical design, that is, the design after mapping has been performed. These constraints are referred to as physical constraints and are defined in the Physical Constraints File (PCF), which is created during mapping.

It is preferable to place any user-generated constraint in the UCF file — not in an NCF or PCF file.

Note: The information in this section applies only to FPGA families.

When a design is mapped, the logical constraints found in the netlist and the UCF file are translated into physical constraints, that is, constraints that apply to a specific architecture. These constraints are found in a mapper-generated file called the Physical Constraints File (PCF). The file contains two sections, the schematic section and the user section. The schematic section contains the physical constraints based on the logical constraints found in the netlist and the UCF file. The user section can be used to add any physical constraints.

Mapping Directives

Mapping directives instruct the mapper to perform specific operations. Following is a linked list of the mapping directives:

AREA_GROUP
BEL
BLKNM
DCI_VALUE
DRIVE
FAST
HBLKNM
HU_SET
IOB
IOBDELAY
IOSTANDARD
KEEP
KEEPER
MAP
NODELAY
OPTIMIZE
PULLDOWN
PULLUP
RLOC
RLOC_ORIGIN
RLOC_RANGE
SAVE NET FLAG
SLEW
U_SET
USE_RLOC
WRITE_MODE
WRITE_MODE_A
WRITE_MODE_B
XBLKNM

Modular Design Constraints

For a complete description of modular design, see the “Modular Design” chapter in the *Development System Reference Guide*.

Overview

Constraints are used to direct the tools for much of the modular design flow. Though these constraints are intended to be generated by the GUI tools (for example, Floorplanner and Constraints Editor), knowledge of these constraints is useful to understand the details of the modular design behavior. A node in the logical hierarchy that has had some constraints applied to it for constraining its location initially defines a module. Constraints can also be applied to locate the boundary or pseudo components for this module, adding more locations to the specified area for other component types and to specify certain module-relative timing constraints.

List of Modular Design Constraints

Following is a linked list of the constraints.

- INST / AREA_GROUP (UCF)
- COMPGRP / COMP (PCF)

- AREA_GROUP / RANGE (UCF)
- COMPGRP / LOCATE (PCF)
- PIN / LOC (UCF)
- COMP / LOCATE (PCF)
- NET / TPSYNC (UCF)
- MODULE / RESYNTHESIZE (UCF)
- COMPGRP / LOCATE (PCF)
- PROHIBIT (PCF)

Placement Constraints

This section describes the placement constraints for each type of logic element, such as flip-flops, ROMs and RAMs, BUFTs, CLBs, IOBs, I/Os, edge decoders, and global buffers in FPGA designs. Individual logic gates, such as AND or OR gates, are mapped into CLB function generators before the constraints are read and therefore cannot be constrained.

Use the following constraints to control mapping and placement of symbols in a netlist.

- BLKNM
- CONFIG (When used with PROHIBIT)
- HBLKNM
- XBLKNM
- LOC
- PROHIBIT
- RLOC
- RLOC_ORIGIN
- RLOC_RANGE

Most constraints can be specified either in the HDL or in the UCF file.

In a constraints file, each placement constraint acts upon one or more symbols. Every symbol in a design carries a unique name, which is defined in the input file. Use this name in a constraint statement to identify the symbol.

The UCF and NCF files are case sensitive. Identifier names (names of objects in the design, such as net names) must exactly match the case of the name as it exists in the source design netlist. However, any Xilinx constraint keyword (for example, LOC, PROHIBIT, RLOC, BLKNM) can be entered in either all upper-case or all lower-case letters. Mixed case is not allowed.

Relative Location (RLOC) Constraints

The RLOC constraint groups logic elements into discrete sets. You can define the location of any element within the set relative to other elements in the set, regardless of eventual placement in the overall design. For example, if RLOC constraints are applied to a group of eight flip-flops organized in a column, the mapper maintains the columnar order and moves the entire group of flip-flops as a single unit. In contrast, absolute location (LOC) constraints constrain design elements to specific locations on the FPGA die with no relation to other design elements.

Placement Constraints

Following is a linked list of all of the placement constraints:

- AREA_GROUP
- BEL
- CONFIG (When used with PROHIBIT)
- LOC
- LOCATE
- OPT_EFFORT
- PROHIBIT
- RLOC
- RLOC_ORIGIN
- RLOC_RANGE
- USE_RLOC

Routing Directives

Routing directives instruct PAR to perform specific operations. Following are the routing directives:

- AREA_GROUP
- CONFIG_MODE
- FILE
- LOCK
- LOCK_PINS
- OPT_EFFORT
- USELOWSKEWLINES

Synthesis Constraints

Synthesis constraints instruct the synthesis tool to perform specific operations. For example, CLOCK_BUFFER selects the type of clock buffer to be inserted on the clock port.

Following is a linked list of the synthesis constraints.

BOX_TYPE
BUFFER_TYPE
BUFG (CPLD)
BUFGCE
CLK_FEEDBACK
CLOCK_BUFFER
CLOCK_SIGNAL
DECODER_EXTRACT
ENUM_ENCODING
EQUIVALENT_REGISTER_REMOVAL
FSM_ENCODING
FSM_EXTRACT
FULL_CASE
INCREMENTAL_SYNTHESIS
IOB
IOSTANDARD
KEEP
KEEP_HIERARCHY
LOC
LUT_MAP
MAP
MAX_FANOUT
MOVE_FIRST_STAGE
MOVE_LAST_STAGE
MULT_STYLE
MUX_EXTRACT
MUX_STYLE
OPT_LEVEL
OPT_MODE
PARALLEL_CASE
PERIOD
PRIORITY_EXTRACT
RAM_EXTRACT
RAM_STYLE
REGISTER_BALANCING
REGISTER_DUPLICATION
REGISTER_POWERUP
RESOURCE_SHARING
RESYNTHESIZE
RLOC
ROM_EXTRACT
ROM_STYLE
SHIFT_EXTRACT
SHREG_EXTRACT
SLEW
SLICE_PACKING
SLICE_UTILIZATION_RATIO
SLICE_UTILIZATION_RATIO_MAXMARGIN
TIG
TRANSLATE_OFF and TRANSLATE_ON
USELOWSKEWLINES
XOR_COLLAPSE

Timing Constraints

Xilinx software enables you to specify precise timing constraints for your Xilinx designs. You can specify the timing constraints for any nets or paths in your design or you can specify them globally. One way of specifying path requirements is to first identify a set of paths by identifying a group of start and end points. The start and end points can be flip-flops, I/O pads, latches, or RAMs. You can then control the worst-case timing on the set of paths by specifying a single delay requirement for all paths in the set.

The primary method of specifying timing constraints is by entering them in your design (HDL and schematic). However, you can also specify timing constraints in constraints files (UCF, NCF, PCF, XCF). For detailed information about each constraint, see later chapters in the book.

Once you define timing specifications and map the design, PAR places and routes your design based on these requirements.

To analyze the results of your timing specifications, use the command line tool, TRACE (TRCE) or the GUI tool Timing Analyzer.

XST Timing Constraints

XST supports an XCF (XST Constraints File) syntax to define synthesis and timing constraints. Please note that starting from 7.1i release the old constraint syntax is not supported any more.

Timing constraints supported by XST can be applied either via the -glob_opt command line switch, which is the same as selecting Global Optimization Goal from the Synthesis Options tab of the Process Properties menu, or via the constraints file.

- Using the -glob_opt or Global Optimization Goal method allows you to apply global timing constraints. These constraints are applied globally to the entire design. You cannot specify a value for these constraints as XST will optimize them for the best performance. Note that these constraints are overridden by constraints specified in the constraints file.
- Using the constraint file method you can use the native UCF timing constraint syntax. Using the XCF syntax, XST supports constraints such as TNM_NET, TIMEGRP, PERIOD, TIG, FROM-TO, including wildcards and hierarchical names.

  Note: Timing constraints are only written to the NGC file when the Write Timing Constraints property is checked in the Process Properties dialog box in Project Navigator, or the *-write_timing_constraints* option is specified when using the command line. By default, they are not written to the NGC file.

Independent of the way timing constraints are specified, the Clock Signal option effects timing constraint processing. In the case where a clock signal goes through combinatorial logic before being connected to the clock input of a flip-flop, XST cannot identify what input pin is the real clock pin. The CLOCK_SIGNAL constraint allows you to define the clock pin. See "CLOCK_SIGNAL" for details.

XCF Timing Constraint Support

IMPORTANT: If you specify timing constraints in the XCF file, Xilinx strongly suggests that you to use the '/' character as a hierarchy separator instead of '_'.

The following timing constraints are supported in the XST Constraints File (XCF).

- **From-To**

  FROM-TO defines a timing constraint between two groups. A group can be user-defined or predefined (FFS, PADS, RAMS). See "FROM-TO" for details.

  Example:

  XCF Syntax:

  ```
  TIMESPEC "TSname"=FROM "group1" TO "group2" value;
  ```

- **Offset**

  OFFSET is a basic timing constraint. It specifies the timing relationship between an external clock and its associated data-in or data-out pin. OFFSET is used only for pad-related signals, and cannot be used to extend the arrival time specification method to the internal signals in a design.

  OFFSET allows you to:

  - Calculate whether a setup time is being violated at a flip-flop whose data and clock inputs are derived from external nets.
  - Specify the delay of an external output net derived from the Q output of an internal flip-flop being clocked from an external device pin.

See "OFFSET" for details.

XCF Syntax:

```
OFFSET = {IN|OUT} "offset_time" [units] {BEFORE|AFTER} "clk_name"
[TIMEGRP "group_name"];
```

- **TIG**

  The TIG constraint causes all paths going through a specific net to be ignored for timing analyses and optimization purposes. This constraint can be applied to the name of the signal affected. See "TIG" for details.

  XCF Syntax:

  ```
  NET "netname" TIG;
  ```

- **TIMEGRP**

  TIMEGRP is a basic grouping constraint. In addition to naming groups using the TNM identifier, you can also define groups in terms of other groups. You can create a group that is a combination of existing groups by defining a TIMEGRP constraint.

  You can place TIMEGRP constraints in a constraints file (XCF or NCF). You can use TIMEGRP attributes to create groups using the following methods.

  - Combining multiple groups into one
  - Defining flip-flop subgroups by clock sense

  See "TIMEGRP" for details.

  XCF Syntax:

  ```
  TIMEGRP "newgroup"="existing_grp1" "existing_grp2"
  ["existing_grp3" . . .];
  ```

- **TNM**

  TNM is a basic grouping constraint. Use TNM (Timing Name) to identify the elements that make up a group which you can then use in a timing specification. TNM tags specific FFS, RAMs, LATCHES, PADS, BRAMS_PORTA, BRAMS_PORTB, CPUS, HSIOS, and MULTS as members of a group to simplify the application of timing specifications to the group.

  The RISING and FALLING keywords may also be used with TNMs. See "TNM" for details.

  XCF Syntax:

  ```
  {NET | PIN} "net_or_pin_name" TNM=[predefined_group:] identifier;
  ```

- **TNM Net**

  TNM_NET is essentially equivalent to TNM on a net *except* for input pad nets. (Special rules apply when using TNM_NET with the PERIOD constraint for Virtex/-E/-II/-II Pro/-II Pro X DLL/DCMs. See "PERIOD Specifications on CLKDLLs and DCMs".)

  A TNM_NET is a property that you normally use in conjunction with an HDL design to tag a specific net. All downstream synchronous elements and pads tagged with the TNM_NET identifier are considered a group. See "TNM" for details.

  XCF Syntax:

  ```
  NET "netname" TNM_NET=[predefined_group:] identifier;
  ```

Timing Model

The timing model used by XST for timing analysis takes into account both logic delays and net delays. These delays are highly dependent on the speed grade that can be specified to XST. These delays are also dependent on the selected technology (for example, Virtex, Virtex-E). Logic delays data are identical to the delays reported by Trce (Timing analyzer after Place and Route). The Net delay model is estimated based on the fanout load.

Priority

Constraints are processed in the following order:

- Specific constraints on signals
- Specific constraints on top module
- Global constraints on top module

For example, constraints on two different domains or two different signals have the same priority (that is, PERIOD clk1 can be applied with PERIOD clk2).

Limitations

If multiple specific constraints are set, XST will stop optimization either when all constraints are satisfied or when optimization does not succeed in satisfying the current most critical constraint.

List of Timing and Grouping Constraints

Following is a linked list of all timing constraints and associated grouping constraints:

ASYNC_REG	OFFSET	TIMESPEC
DISABLE	ONESHOT	TNM
DROP_SPEC	PERIOD	TNM_NET
ENABLE	PRIORITY	TPSYNC
FROM-THRU-TO	TEMPERATURE	TPTHRU
FROM-TO	TIG	TSidentifier
MAXSKEW	TIMEGRP	VOLTAGE

Chapter 3

Entry Strategies for Xilinx Constraints

The following sections describe various methods for entering constraints.

- Schematic Designs
- VHDL
- Verilog
- ABEL
- UCF
- PCF Files
- NCF
- Constraints Editor
- Constraint Files for XST: XCF
- XST Command Line
- Project Navigator
- Floorplanner
- PACE
- FPGA Editor
- Constraints Priority
- Constraint Entry Table

Schematic Designs

You can add Xilinx constraints as attributes within a symbol or schematic drawing. Constraints are added following these rules.

- If a constraint applies to a net, you add it as an attribute to the net.
- If a constraint applies to an instance, you add it as an attribute to the instance.
- You cannot add global constraints such as PART and PROHIBIT.
- You cannot add any timing specifications that would be attached to a TIMESPEC or TIMEGRP.
- Attribute names and values must be entered in either all upper case or all lower case—no mixed upper and lower case.

Refer to the Schematic and Symbol Editors online help procedures for creating, modifying, and displaying attributes. These online help topics are:

- Adding an Attribute
- Changing an Attribute Value

- Displaying Attributes on a Schematic
- Displaying Attributes on a Symbol

In the *Constraints Guide*, the syntax for any constraint that can be entered in an schematic is described in the individual section for the constraint. For example, to see the proper schematic syntax for the BEL constraint, go to "Schematic" in the BEL section.

For a list of supported constraints, see "Constraint Entry Table".

VHDL

In VHDL code, constraints can be described with VHDL attributes. Before it can be used, a constraint must be declared with the following syntax:

```
attribute attribute_name : string;
```

Example:

```
attribute RLOC : string;
```

An attribute can be declared in an entity or architecture. If declared in the entity, it is visible both in the entity and the architecture body. If the attribute is declared in the architecture, it cannot be used in the entity declaration. Once declared you can specify a VHDL attribute as follows:

```
attribute attribute_name of
{component_name|label_name|entity_name|signal_name
|variable_name|type_name}: {component|label|entity|signal
|variable|type} is attribute_value;
```

Accepted *attribute_values* depend on the attribute type.

Examples:

```
attribute RLOC of u123 : label is "R11C1.S0";
attribute bufg of my_clock: signal is “clk”;
```

For Xilinx, the most common objects are **signal**, **entity**, and **label**. A label describes an instance of a component.

VHDL is case insensitive.

For a list of supported constraints, see "Constraint Entry Table".

Please note that in some cases existing Xilinx constraints could not be used in attributes, because they are VHDL key words at the same time. In order to avoid this problem you may use a constraint alias approach introduced in 7.1i release. Starting form 7.1i release each constraint has its own alias. The alias name is based on the original constraint name with starting prefix "XIL_". For example a "RANGE" constraint could not be used in attribute directly. You have to use "XIL_RANGE" instead.

Verilog

You can specify constraints as follows in Verilog code:

```
 // synthesis attribute attribute_name [of]
{module_name|instance_name|signal_name}[is] attribute_value;
```

The *module_name*, *instance_name*, *signal_name*, and *attribute_value* are case sensitive.

Example:

```
// synthesis attribute RLOC of u123 is R11C1.S0;
// synthesis attribute HU_SET u1 MY_SET;
// synthesis attribute bufg of my_clock is “clk”;
```

The PARALLEL_CASE, FULL_CASE, and TRANSLATE_OFF and TRANSLATE_ON directives follow a different syntax. See the section for each of these individual constraints for the specific syntax.

For a list of supported constraints, see “Constraint Entry Table”.

ABEL

Xilinx supports the use of ABEL for CPLD devices.

Following is an example of the basic syntax.

```
XILINX PROPERTY 'bufg=clk my_clock';
```

For a list of supported constraints, see “Constraint Entry Table”.

UCF

The UCF file is an ASCII file specifying constraints on the logical design. You create this file and enter your constraints in the file with a text editor.

You can also use the Constraints Editor to create constraints within a UCF file. See “Constraints Editor” for details.

These constraints affect how the logical design is implemented in the target device. You can use the file to override constraints specified during design entry.

For a list of supported constraints, see “Constraint Entry Table”.

UCF Flow

The following figure illustrates the UCF flow.

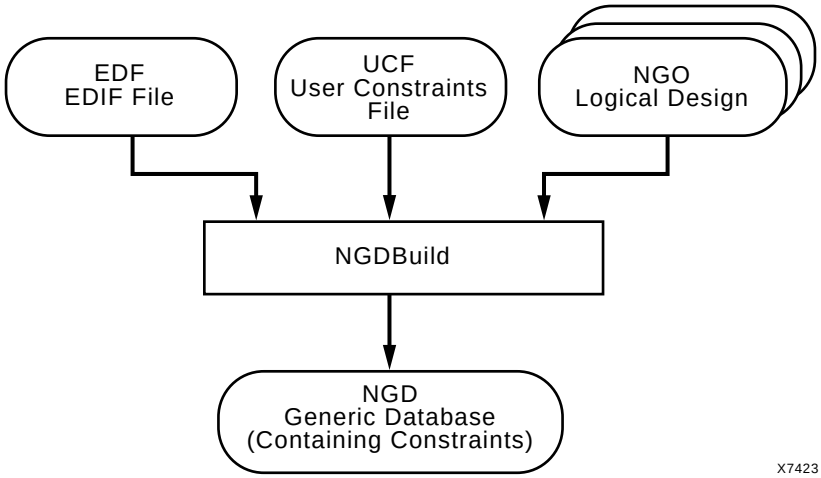


Figure 3-1: **UCF File Flow**

The UCF file is an input to NGDBuild (see the preceding figure). The constraints in the UCF file become part of the information in the NGD file produced by NGDBuild. For

FPGAs, some of these constraints are used when the design is mapped by MAP and some of the constraints are written into the PCF (Physical Constraints File) produced by MAP.

The constraints in the PCF file are used by each of the physical design tools (for example, PAR and the timing analysis tools), which are run after your design is mapped.

Manual Entry of Timing Constraints

You can manually enter timing specifications as constraints in a UCF file. When you then run NGDBuild on your design, your timing constraints are added to the design database as part of the NGD file.

To avoid manually entering timing constraints in a UCF file, use the Constraints Editor, a tool that greatly simplifies constraint creation. For a detailed description of how to use the editor, see the Constraints Editor online help.

UCF/NCF File Syntax

Logical constraints are found in:

- a Netlist Constraint File (NCF), an ASCII file generated by synthesis programs
- User Constraint File (UCF), an ASCII file generated by the user

This section describes the rules for entering constraints in a UCF or NCF file.

It is preferable to place any user-generated constraint in the UCF file — *not* in an NCF or PCF file.

General Rules

Following are some general rules for the UCF and NCF files.

- The UCF and NCF files are case sensitive. Identifier names (names of objects in the design, such as net names) must exactly match the case of the name as it exists in the source design netlist. However, any Xilinx constraint keyword (for example, LOC, PERIOD, HIGH, LOW) may be entered in all upper-case, all lower-case, or mixed case.
- Each statement is terminated by a semicolon (;).
- No continuation characters are necessary if a statement exceeds one line, since a semicolon marks the end of the statement.
- It is recommended to group similar blocks, or components, under a timing constraint and not to separate timing constraints.
- You can add comments to the UCF / NCF file by beginning each comment line with a pound (#) sign. Following is an example of part of a UCF / NCF file containing comments.

  ```
  # file TEST.UCF
  # net constraints for TEST design
  NET “$SIG_0“ MAXDELAY = 10;
  NET “$SIG_1“ MAXDELAY = 12 ns;
  ```

  C and C++ style comments (`/* */` and respectively) are also supported.
- Statements do not have to be placed in any particular order in the UCF / NCF file.
- Although not required, Xilinx recommends that NET and INST names be enclosed in double quotes to avoid errors. Additionally, inverted signal names that contain a tilde, for example, ~OUTSIG1, must always be enclosed in double quotes.

- You can enter multiple constraints for a given instance. See "Entering Multiple Constraints".

Conflict in Constraints

The constraints in the UCF / NCF files and the constraints in the schematic or synthesis file are applied equally. It does not matter whether a constraint is entered in the schematic or synthesis file or in the UCF / NCF files. If the constraints overlap, UCF overrides NCF and schematic constraints. NCF overrides schematic constraints.

If by mistake two or more elements are locked onto a single location, the mapper detects the conflict, issues a detailed error message, and stops processing so that you can correct the mistake.

Syntax

The UCF file supports a basic syntax that can be expressed as:

```
{NET|INST|PIN} "full_name" constraint;
```

or as

```
SET set_name set_constraint;
```

where

- *full_name* is a full hierarchically qualified name of the object being referred to. When the name refers to a pin, the instance name of the element is also required.
- *constraint* is a constraint in the same form as it would be used if it were attached as an attribute on a schematic object. For example, LOC=P38 or FAST, and so forth.
- *set_name* is the name of an RLOC set. See "RLOC Description" for more information.
- *set_constraint* is an RLOC_ORIGIN or RLOC_RANGE constraint

Specifying Attributes for TIMEGRP and TIMESPEC

To specify attributes for TIMEGRP, the keyword TIMEGRP precedes the attribute definitions in the constraints files.

```
TIMEGRP "input_pads"=pads EXCEPT output_pads;
```

Using Reserved Words

In all of the constraints files (NCF, UCF, and PCF), instance or variable names that match internal reserved words may be rejected unless the names are enclosed in double quotes. It is good practice to enclose all names in double quotes.

For example, the following entry would not be accepted because the word net is a reserved word.

```
NET net OFFSET=IN 20 BEFORE CLOCK;
```

Following is the recommended way to enter the constraint.

```
NET "net" OFFSET=IN 20 BEFORE CLOCK;
```

or

```
NET "$SIG_0" OFFSET=IN 20 BEFORE CLOCK;
```

Inverted signal names, for example ~OUTSIG1, must always be enclosed in double quotes as shown in the following example.

```
NET “~OUTSIG1” OFFSET=IN 20 BEFORE CLOCK;
```

Wildcards

You can use the wildcard characters, * and ?, in constraint statements as follows:

- The asterisk (*) represents any string of zero or more characters
- The question mark (?) indicates a single character

In net names, the wildcard characters enable you to select a group of symbols whose output net names match a specific string or pattern. For example, the following constraint increases the output speed of the pads to which nets with names that begin with any series of characters followed by "AT" and end with one single character are connected.

```
NET “*AT?” FAST;
```

In an instance name, a wildcard character by itself represents every symbol of the appropriate type. For example, the following constraint initializes an entire set of ROMs to a particular hexadecimal value, 5555.

```
INST “$1I3*/ROM2” INIT=5555;
```

If the wildcard character is used as part of a longer instance name, the wildcard represents one or more characters at that position.

In a location, you can use a wildcard character for either the row number or the column number. For example, the following constraint specifies placement of any instance under the hierarchy of loads_of_logic in any CLB in column 8.

```
INST “/loads_of_logic/*” LOC=CLB_r*c8;
```

Wildcard characters can be used in dot extensions.

```
CLB_R1C3.*
```

Wildcard characters cannot be used for both the row number and the column number in a single constraint, since such a constraint is meaningless.

Traversing Hierarchies

Top-level block names (design names) are ignored when searching for instance name matches.

You can use the asterisk wildcard character (*) to traverse the hierarchy of a design within a UCF or NCF file. The following syntax applies (where level1 is an example hierarchy level name).

*	Traverses all levels of the hierarchy
level1/*	Traverses all blocks in level1 and below
level1/*/	Traverses all blocks in the level1 hierarchy level but no further

Consider the following design hierarchy.

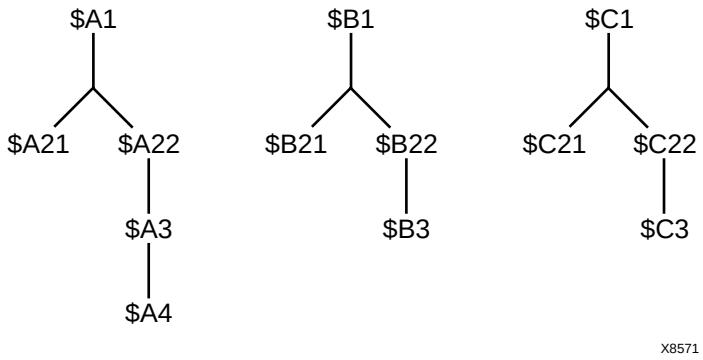


Figure 3-2: **UCF Design Hierarchy**

With the example design hierarchy, the following specifications illustrate the scope of the wildcard.

```
INST *          => <everything>
INST /*         => <everything>
INST /*/        => <$A1,$B1,$C1>
INST $A1/*      => <$A21,$A22,$A3,$A4>
INST $A1/*/     => <$A21,$A22>
INST $A1/*/*    => <$A3,$A4>
INST $A1/*/*/   => <$A3>
INST $A1/*/*/*  => <$A4>
INST $A1/*/*/*/ => <$A4>
INST /*/*22/    => <$A22,$B22,$C22>
INST /*/*22     => <$A22,$A3,$A4,$B22,$B3,$C3>
```

Entering Multiple Constraints

You can cascade multiple constraints for a given instance in the UCF file:

INST *instanceName constraintName* **=** *constraintValue* **|** *constraintName* **=** *constraintValue*;

For example:

```
INST myInst LOC = P53 | IOSTANDARD = LVPECL33 | SLEW = FAST;
```

File Name

By default, NGDBuild reads the constraints file that carries the same name as the input design with a .ucf extension. However, you can specify a different constraints file name with the **-uc** option when running NGDBuild. NGDBuild automatically reads in the NCF file if it has the same base name as the input EDIF file and is in the same directory as the EDIF file.

The implementation tools (NGDBuild, MAP, PAR, etc.) require file name extensions in all lowercase (.ucf, for example) in command lines.

Instances and Blocks

Because the statements in the constraints file concern instances and blocks, these entities are defined here.

- An *instance* is a symbol on the schematic.
- An *instance name* is the symbol name as it appears in the EDIF netlist.
- A *block* is a CLB, an IOB, or a TBUF.
- You can specify the *block name* by using the BLKNM, HBLKNM, or the XBLKNM attribute; by default, the software assigns a block name on the basis of a signal name associated with the block.

PCF Files

The NGD file produced when a design netlist is read into the Xilinx Development System may contain a number of logical constraints. These constraints originate in any of these sources.

- An attribute assigned within a schematic or HDL file.
- A constraint entered in a UCF (User Constraints File).
- A constraint appearing in an NCF (Netlist Constraints File) produced by a CAE vendor toolset.

Logical constraints in the NGD file are read by MAP. MAP uses some of the constraints to map the design and converts logical constraints to physical constraints. MAP then writes these physical constraints into a Physical Constraints File (PCF).

The PCF file is an ASCII file containing two separate sections: a section for those physical constraints created by the mapper and a section for physical constraints entered by the user. The mapper section is rewritten every time you run the mapper. Mapper-generated physical constraints appear first in the file, followed by user physical constraints. This order dictates that in the event of conflicts between mapper-generated and user constraints, user constraints are the last-read and override mapper-generated constraints.

The mapper-generated section of the file is preceded by a **SCHEMATIC START** notation on a separate line. The end of this section is indicated by **SCHEMATIC END**, also on a separate line. User-generated constraints, such as timing constraints, should always be entered after **SCHEMATIC END**.

You can write user constraints directly into the file or you can write them indirectly (or undo them) from within the FPGA Editor. (For more information on constraints in the FPGA Editor, see the FPGA Editor online help).

Note: Whenever possible, you should add design constraints to the HDL, schematic, or UCF, instead of PCF. This simplifies design archiving and improves design role checking.

The PCF file is an optional input to PAR, the FPGA Editor, TRACE, NetGen, and BitGen.

The file may contain any number of constraints and any number of comments in any order. A comment consists of either a pound sign (#) or double slashes (//) followed by any number of other characters up to a new line. Each comment line must begin with # or / /.

For a list of supported constraints, see "Constraint Entry Table".

The structure of the PCF file is as follows.

```
schematic start;
translated schematic and UCF or NCF constraints in PCF format
```

```
schematic end;
user-entered physical constraints
```

You should put all user-entered physical constraints after the “schematic end” statement. *Any constraints preceding this section or within this section may be overwritten or ignored.*

Do not edit the schematic constraints. They are overwritten every time the mapper generates a new PCF file.

Global constraints need not be attached to any object but should be entered in a constraints file.

The end of each constraint statement must be indicated with a semi-colon.

In all of the constraints files (NCF, UCF, and PCF), instance or variable names that match internal reserved words will be rejected unless the names are enclosed in double quotes. It is good practice to enclose all names in double quotes. For example, the following entry would not be accepted because the word net is a reserved word.

```
NET net FAST;
```

Following is the recommended way to enter the constraint.

```
NET “net” FAST;
```

NCF

The syntax rules for NCF files are the same as those for the UCF file. See “UCF / NCF File Syntax”.

For a list of supported constraints, see “Constraint Entry Table”.

Constraints Editor

The Constraints Editor is a graphical user interface (GUI) tool for entering timing constraints and pin location constraints. The user interface simplifies constraint entry by guiding you through constraint creation without your needing to understand UCF file syntax.

Used in the implementation phase of the design after the translation step (NGDBuild), the Constraints Editor allows you to create and manipulate constraints without any direct editing of the UCF. After the constraints are created or modified with the Constraints Editor, NGDBuild must be run again, using the new UCF and design source netlist files as input and generating a new NGD file as output.

The Constraints Editor interface consists of a main window, four tab windows, a constraints window, an output window, and numerous dialog boxes. For a description of these windows, refer to the Constraints Editor online help. For a description of how to use the editor to create constraints, refer to the Procedures in the Constraints Editor online help.

For a list of supported constraints, see “Constraint Entry Table”.

Input/Output Files

The Constraints Editor requires a User Constraints File (UCF), a Xilinx Constraints File (XCF), and a Native Generic Database (NGD) file. The Constraints Editor uses the NGD to provide names of logical elements for grouping. As output, it uses the UCF.

After you open the Constraints Editor, you must first open a UCF file. If the UCF and NGD root names are not the same, you must select the appropriate NGD file to open. For details on loading files, see the "Loading Files" topic in the Constraints Editor online help.

Upon successful completion, the Constraints Editor writes out a UCF. NGDBuild (translation) uses the UCF, along with design source netlists, to produce an NGD file. The NGD file is read by the MAP program. MAP generates a physical design database in the form of an NCD (Native Circuit Description) file and also generates a PCF (Physical Constraints File). The implementation tools use these files to ultimately produce a bitstream.

In this software release, not all Xilinx constraints are accessible through this GUI. Constraints supported in the GUI and the associated UCF syntax are described in "UCF Syntax".

Starting the Constraints Editor

The Constraints Editor runs on PCs and workstations. You can start it from within the Project Navigator, as a standalone, or from the command line.

From the Project Navigator

Within the Project Navigator, you can launch the Constraints Editor from the Processes window. First select a design file in the Sources window. Then double-click Create Timing Constraints in the Processes window, which is located within User Constraints underneath Design Utilities.

As a Standalone

If you installed the Constraints Editor as a standalone tool on the PC, click the Constraints Editor icon on the Windows desktop or select **Start** → **Programs** → **Xilinx ISE 6**→ **Accessories** → **Constraints Editor**.

From the Command Line

To start the Constraints Editor from the UNIX or DOS command prompt with no data loaded into the editor, type the following command.

```
constraints_editor
```

Below are variations for starting the Constraints Editor from the command line.

The following command starts the Constraints Editor with the given NGD file loaded. If a UCF file with the same base name as the NGD file exists, it will be loaded also. Otherwise, you will be prompted for a UCF file.

```
constraints_editor ngdfile_name
```

where *ngdfile_name* is the name of the NGD file. It is not necessary to use the .ngd extension.

The following command starts the Constraints Editor with the NGD file and the UCF file loaded into the editor.

```
constraints_editor ngdfile_name -uc ucf_file_name
```

where *ngdfile_name* is the name of the NGD file and *ucf_file_name* is the name of the UCF file. It is not necessary to use the .ucf extension.

To run the tool as a background process on a workstation, type the following.

```
constraints_editor &
```

Obtaining Online Help

The Constraints Editor contains a Help menu. You can obtain help on commands and procedures through the Help menu or by selecting the Help toolbar button. In addition, the dialog boxes associated with many commands have a Help button that you can click to obtain context-sensitive help.

Exiting the Constraints Editor

To exit, select **File** → **Exit**. A confirmation dialog box appears. If you have unsaved data, you are asked whether you want to save it. Click **Yes** to save the data and quit the application.

UCF Syntax

This section describes the UCF syntax for constraints that are supported by the Constraints Editor. For a comprehensive discussion on setting these constraints in the Constraints Editor, refer to the Constraints Editor online help.

Group Elements Associated by Nets (TNM_Net)

Definition

A TNM_NET (timing name for nets) is an attribute that can be used to identify the elements that make up a group which can then be used in a timing specification. Essentially TNM_NET is equivalent to TNM on a net except for pad nets.

UCF Syntax

```
NET “netname” TNM_Net=identifier;
```

netname is the name of a net. *identifier* is a value that consists of any combination of letters, numbers, or underscores.

Group Elements by Instance Name (TNM)

Definition

Identifies the instances that make up a group which can then be used in a timing specification. A TNM (pronounced tee-name) is a flag that you place directly on your schematic to tag a specific net, element pin, primitive or macro. All symbols tagged with the TNM identifier are considered a group.

UCF Syntax

```
INST “instance_name” TNM=identifier;
```

instance_name can be FFs, All Pads, Input Pads, Output Pads, Bi-directional Pads, 3-stated Output Pads, RAMs, or Latches.

identifier is a value that consists of any combination of letters, numbers, or underscores. Keep it short for convenience and clarity.

Group Elements by Element Output Net Name Schematic Users (TIMEGRP)

Definition

Specifies a new group with instances of FFs, PADs, RAMs, LATCHES, or User Groups by output net name.

UCF Syntax

```
TIMEGRP identifier=element (output_netname);
```

identifier is the name for the new time group.

element can be FFS, All Pads, Input Pads, Output Pads, Bi-directional Pads, 3-stated Output Pads, RAMs, LATCHES, or User Groups.

output_netname is the name of the net attached to the element.

Timing THRU Points (TPTHRU)

Definition

Identifies an intermediate point on a path.

UCF Syntax

```
INST "instance_name" TPTHRU=identifier;
NET "netname" TPTHRU=identifier;
```

identifier is a unique name.

Pad to Setup

Definition

Specifies the timing relationship between an external clock and data at the pins of a device. Operates on pads or predefined groups of pads.

UCF Syntax

```
OFFSET=IN time unit BEFORE pad_clock_netname [TIMEGRP
"reg_group_name"];
[NET "pad_netname"] OFFSET=IN time unit BEFORE pad_clock_netname
[TIMEGRP "reg_group_name"];
[TIMEGRP "padgroup_name"] OFFSET=IN time unit BEFORE pad_clock_netname
[TIMEGRP "reg_group_name"];
```

padgroup_name is the name of a group of pads predefined by the user.

reg_group_name is the name of a group of registers predefined by the user.

pad_clock_netname is the name of the clock at the port.

For more information on Pad to Setup, see the discussion of the Global Tab window in the Constraints Editor online help.

Clock to Pad

Definition

Specifies the timing relationship between an external clock and data at the pins of a device. Operates on pads or predefined groups of pads.

UCF Syntax

```
OFFSET=OUT time unit AFTER pad_clock_netname [TIMEGRP
"reg_group_name"];
NET "pad_netname" OFFSET=OUT time unit AFTER pad_clock_netname [TIMEGRP
"reg_group_name"];
TIMEGRP "padgroup_name" OFFSET=OUT time unit AFTER pad_clock_netname
[TIMEGRP "reg_group_name"];
```

padgroup_name is the name of a group of pads predefined by the user.

reg_group_name is the name of a group of registers predefined by the user.

pad_clock_netname is the name of the clock at the port.

For more information on Clock to Pad, see the discussion of the Global Tab window in the Constraints Editor online help.

Slow/Fast Path Exceptions (FROM TO)

Definition

Establishes an explicit maximum acceptable time delay between groups of elements.

UCF Syntax

```
TIMESPEC "TSid"=FROM "source_group" TO "destination_group" time [unit];
```

source_group and *destination_group* are FFS, RAMS, PADS, LATCHES, or user-created groups.

Multicycle Paths (FROM/THRU/TO)

Definition

Establishes a maximum acceptable time delay between groups of elements relative to another timing specification.

UCF Syntax

```
TIMESPEC "TSid"=FROM "source_group" THRU "timing_point" TO
"destination_group" time [unit];
```

source_group and *destination_group* are FFS, RAMS, PADS, LATCHES, or user-created groups.

timing_point is an intermediate point as specified by the TPTHRU constraint on the Advanced tab window.

False Paths (FROM TO TIG)

Definition

Marks paths between a source group and a destination group that are to be ignored for timing purposes.

UCF Syntax

```
TIMESPEC "TSid"=FROM "source_group" TO "destination_group" TIG;
TIMESPEC "TSid"=FROM "source_group" THRU "timing_point(s)" TO
"destination_group" TIG;
```

source_group and *destination_group* are FFS, RAMS, PADS, LATCHES, or user-created groups.

timing_point is an intermediate point as specified by the TPTHRU Points constraint on the Advanced tab window.

False Paths by Net (Net TIG)

Definition

Marks nets that are to be ignored for timing purposes.

UCF Syntax

```
NET "netname" TIG;
NET "netname" TIG="TSid1" ... "TSidn";
```

Period

Definition

Defines a clock period.

UCF Syntax

```
TIMESPEC "TSid"=PERIOD {timegroup_name time | TSid
[+/- phase [units]} [HIGH | LOW high_or_low_time unit];
```

id is a unique identifier. The identifier can consist of letters, numbers, or the underscore character (_).

unit is picoseconds, nanoseconds, microseconds, or milliseconds.

HIGH | **LOW** indicates the state of the first pulse of the clock.

phase is the amount of time that the clock edges are offset when describing the time requirement as a function of another clock.

units are in ms, us, ns, and ps.

Location

Definition

Locks a user-defined port to a device pin.

UCF Syntax

```
NET "pad_netname" LOC=location;
```

location is a device pin identification, for example, P10.

Prohibit I/O Locations

Definition

Disallows the use of an I/O site by PAR (Place and Route) and FPGA Editor.

UCF Syntax

```
CONFIG PROHIBIT=location1, [location2,... locationn];
```

location is a pin location identification.

FAST/SLOW

Definition

Assigns a slew rate to a selected port.

UCF Syntax

```
Net "port_netname" {FAST|SLOW};
```

port_netname is the name of the port.

PULLUP/PULLDOWN

Definition

Signifies a pull level (PULLUP, PULLDOWN, or KEEPER) for a selected output port. KEEPER is used for Virtex devices only. When a 3-state buffer goes to high impedance, KEEPER keeps the input level of the buffer on the pad net.

UCF Syntax

```
NET "port_netname" {PULLUP| PULLDOWN |KEEPER};
```

port_netname is the name of the net attached to the port.

DRIVE

Definition

This constraint assigns a signal strength to a selected port.

UCF Syntax

```
NET "port_netname" DRIVE=value;
```

port_netname is the name of the net attached to the port.

value is drive strength (in mA). Values vary for different devices.

IOSTANDARD (Virtex devices only)

Definition

Assigns an input/output standard to a selected net attached to the port.

UCF Syntax

```
NET "port_netname" IOSTANDARD=standard_name;
```

port_netname is the name of the net attached to the port.

standard_name is the name of the I/O standard (LVTTL, LVCMOS, and so forth).

VOLTAGE

Definition

Allows you to specify operating voltage. This constraint provides a means of prorating delay characteristics based on the specified voltage.

UCF Syntax

```
VOLTAGE=value[units];
```

value is an integer or real number specifying the voltage in volts and *units* is an optional parameter specifying the unit of measure.

TEMPERATURE

Definition

Allows the specification of the operating temperature which provides a means of prorating device delay characteristics based on the specified junction temperature. Prorating is a linear scaling operation on existing speed file delays and is applied globally to all delays.

UCF Syntax

```
TEMPERATURE=value [units];
```

value is an integer or real number specifying the temperature in Celsius as the default. F and K are also accepted.

Constraint Files for XST: XCF

XST supports an XCF syntax to define synthesis and timing constraints. Xilinx strongly suggests that you use the new syntax style for your new devices. The XCF must have an extension of .xcf. Please note that if the extension is not .xcf, XST interprets it as the wrong constraint style.

XCF Specification

The constraint file can be specified in ISE, by going to the Synthesis Process Properties, clicking the XST Synthesis Options tab, clicking the Synthesis Constraint File menu item, and typing the constraint file name. Also, to quickly enable or disable the use of a constraint file by XST, you can check or uncheck the Use Synthesis Constraint File menu item in this same menu. By selecting this menu item, you invoke the -iuc command line switch.

To specify the constraint file in command line mode, use the -uc switch with the *run* command. See Chapter 8, "Command Line Mode," in the *XST User Guide* for details on the **run** command and running XST from the command line.

XCF Syntax and Utilization

The XCF syntax allows you to specify a specific constraint for the entire device (globally) or for specific modules in your design. The syntax is basically the same as the UCF syntax for applying constraints to nets or instances, but with an extension to the syntax to allow constraints to be applied to specific levels of hierarchy. The keyword MODEL defines the entity or module that the constraint will be applied to. If a constraint is applied to an entity or module the constraint will be applied to the each instance of the entity or module.

In general, you should define constraints within the ISE properties dialog (or the XST run script, if running on the command line), then use the XCF file to specify exceptions to these general constraints. The constraints specified in the XCF file will be applied *only* to the module listed, and not to any submodules below it.

To apply a constraint to the entire entity or module use the following syntax:

```
MODEL entityname constraintname = constraintvalue;
```

Examples:

```
MODEL top mux_extract = false;
MODEL my_design max_fanout = 256;
```

Note: If the entity my_design is instantiated several times in the design, the max_fanout=256 constraint is applied to the each instance of my_design.

To apply constraints to specific instances or signals within an entity or module, use the INST or NET keywords:

```
BEGIN MODEL entityname
   INST instancename constraintname = constraintvalue;
   NET signalname constraintname = constraintvalue;
END;
```

Examples:

```
BEGIN MODEL crc32
   INST stopwatch opt_mode = area;
   INST U2 ram_style = block;
   NET myclock clock_buffer = true;
   NET data_in iob = true;
END;
```

See "Constraints Summary," in the *XST User Guide* for the complete list of synthesis constraints that can be applied for XST.

Native vs. Non-Native UCF Constraints Syntax

From a UCF Syntax point of view, all constraints supported by XST can be divided into two groups: native and non-native UCF constraints. Only Timing constraints use native UCF syntax.

For all non-native UCF constraints, the MODEL or BEGIN MODEL... END; constructs must be used. This is true for pure XST constraints such as FSM_EXTRACT or

RAM_STYLE, as well as for implementation non-timing constraints, such as RLOC or KEEP.

For native UCF constraints, such as TNM_NET, TIMEGRP, PERIOD, TIG, FROM-TO, XST supports native UCF syntax, including the use of wildcards and hierarchical names. Do not use these constraints inside the BEGIN MODEL... END construct, otherwise XST issues an error.

IMPORTANT: If you specify timing constraints in the XCF file, Xilinx strongly suggests that you to use '/' character as a hierarchy separator instead of '_' one.

Limitations

When using the XCF syntax, the following limitations exist:

- Nested model statements are not supported in the current release.
- Instance or signal names listed between the BEGIN MODEL statement and the END statement, are only the ones visible inside the entity. Hierarchical instance or signal names are not supported.
- Wildcards in instance and signal names are not supported, except in timing constraints.
- Not all timing constraints are supported in the current release. Refer to "Constraint Entry Table" for more information.

XST Command Line

Several constraints may be accessed via the command line options. The easiest way is to define command line options in a script file and then invoke the script file from the command line.

Following is an example of a script file, foo.scr, with two constraints defined, opt_mode and opt_level.

```
run
-ifn tt1.vhd
-ifmt mixed
-opt_mode SPEED
-opt_level 1
-ofn tt1.ngc
-family virtex2
```

This script file can be executed under XST using the following command:

- Workstation

```
xst -ifn foo.scr
```

You can also generate a log file with the following command:

- Workstation

```
xst -ifn foo.scr -ofn foo.log
```

For a list of supported constraints, see "Constraint Entry Table".

Project Navigator

This section explains how to set synthesis and implementation constraints.

Setting Synthesis Constraints

This section explains how to set global constraints and options from the Process Properties dialog box within the Project Navigator.

Except for the Value fields with check boxes, there is a pulldown arrow or browse button in each Value field. However, you cannot see the arrow until you click in the Value field.

Note: In the following sections, you need to set the Property Display Level to "Advanced" to see all the possible options available. This selection is made within each Process Properties dialog box.

For a list of supported constraints, see "Constraint Entry Table".

Synthesis Options

In order to specify the HDL synthesis options from the Project Navigator:

1. Select a source file from the Source file window.
2. Right click Synthesize in the Process window.
3. Select **Properties**.
4. When the Process Properties dialog box displays, click the Synthesis Options tab.

   Depending on the HDL language (VHDL or Verilog) and the device family you have selected (FPGA or CPLD), one of four dialog boxes displays:

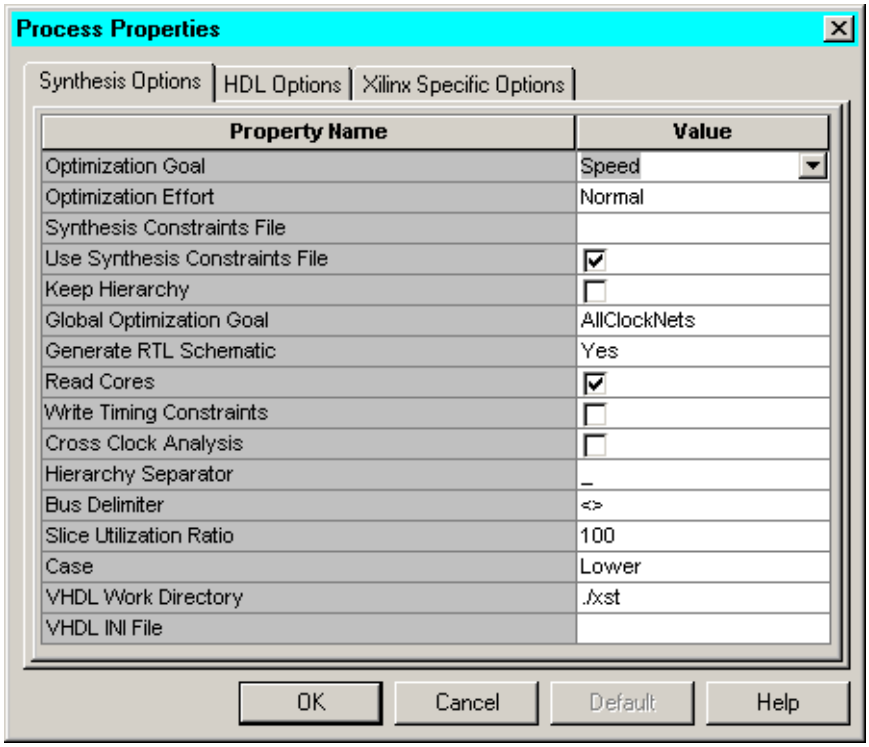


Figure 3-3: **Synthesis Options (VHDL and FPGA)**

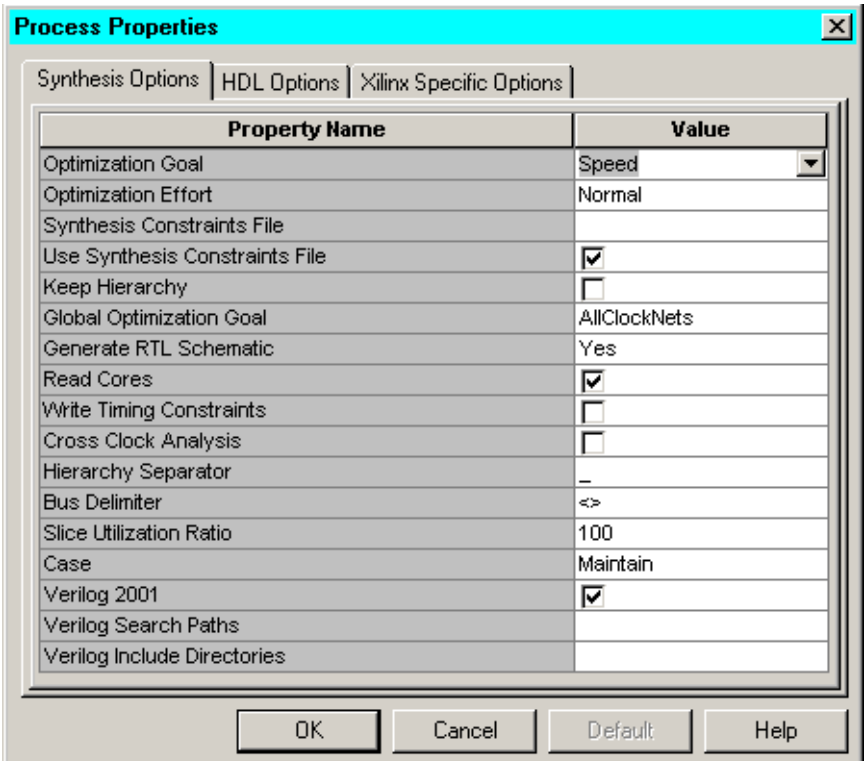


Figure 3-4: **Synthesis Options (Verilog and FPGA)**

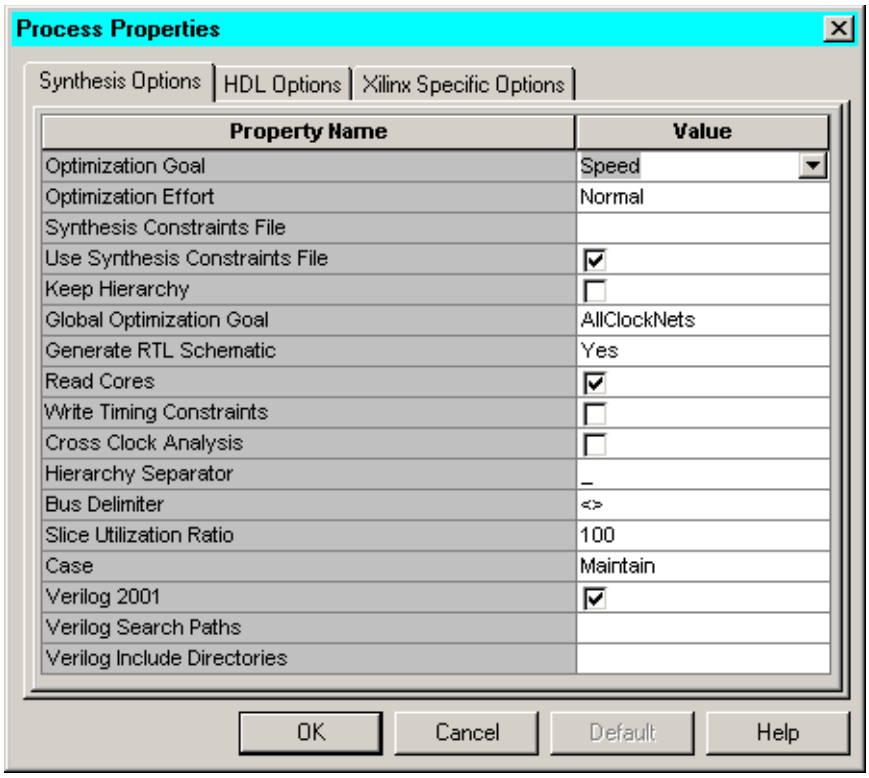


Figure 3-5: **Synthesis Options (Verilog and CPLD)**

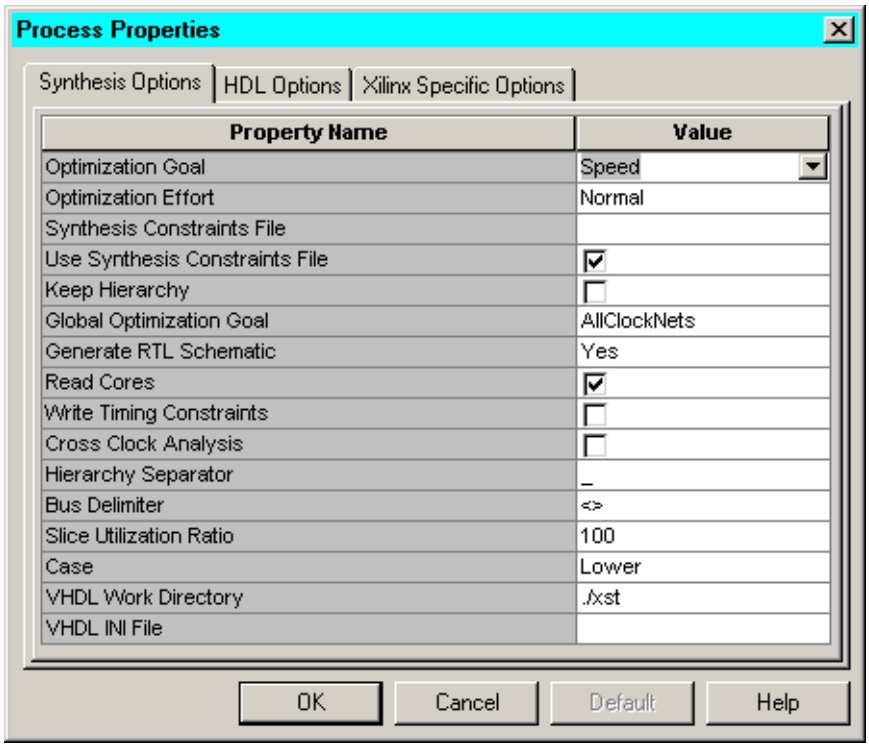


Figure 3-6: **Synthesis Options (VHDL and CPLD)**

The following constraints can be selected from the dialog boxes:

- Optimization Goal
  See "OPT_MODE".
- Optimization Effort
  See "OPT_LEVEL".
- Keep Hierarchy
  See "KEEP_HIERARCHY".
- Slice Utilization Ratio (FPGA Only)
  See the "SLICE_UTILIZATION_RATIO".
- Slice Utilization Ratio Maxmargin (FPGA Only)
  See "SLICE_UTILIZATION_RATIO_MAXMARGIN".

HDL Options

With the Process Properties dialog box displayed for the Synthesize process, select the HDL Option tab. The following dialog box displays.

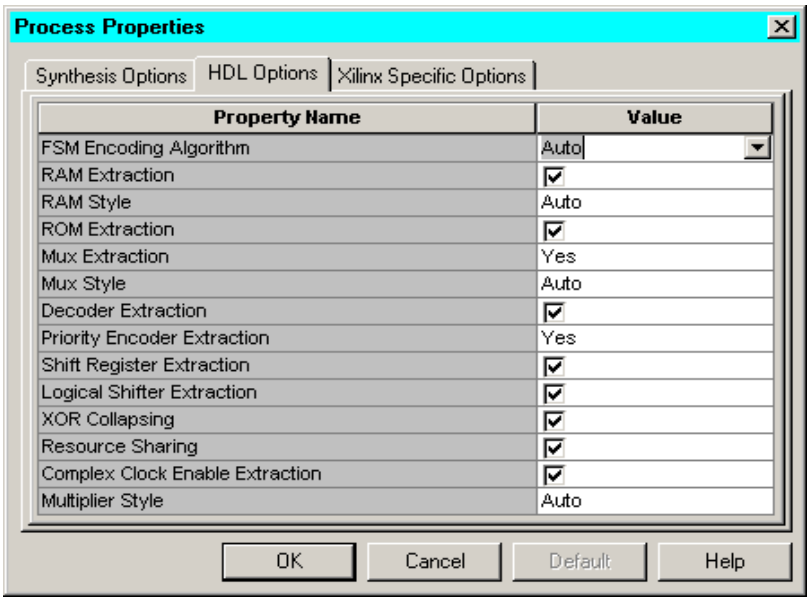


Figure 3-7: **HDL Options Tab**

Some of the HDL Options cannot be set within the Process Properties dialog box. Following is a list of all HDL Options—including those that cannot be set within the HDL Options tab of the Process Properties dialog box:

- FSM Encoding Algorithm
  See "FSM_ENCODING".
- RAM Extraction
  See "RAM_EXTRACT"
- RAM Style
  See "RAM_STYLE".
- ROM Extraction
  See "ROM_EXTRACT".
- Mux Extraction
  See "MUX_EXTRACT".
- Mux Style
  See "MUX_STYLE".
- Decoder Extraction
  See "DECODER_EXTRACT".
- Priority Encoder Extraction
  See "PRIORITY_EXTRACT".
- Shift Register Extraction
  See "SHREG_EXTRACT".
- Logical Shifter Extraction
  See "SHIFT_EXTRACT".
- XOR Collapsing
  See "XOR_COLLAPSE".
- Resource Sharing
  See "RESOURCE_SHARING".

Xilinx Specific Options

From the Process Properties dialog box for the Synthesize process, select the Xilinx Specific Options tab to display the options.

Depending on the device family, one of the following dialog boxes displays:

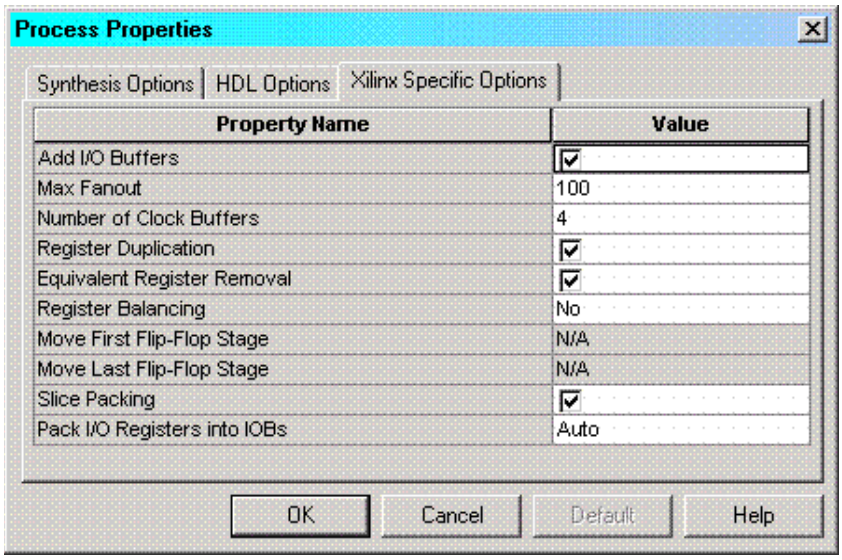


Figure 3-8: **Xilinx Specific Options (FPGAs)**

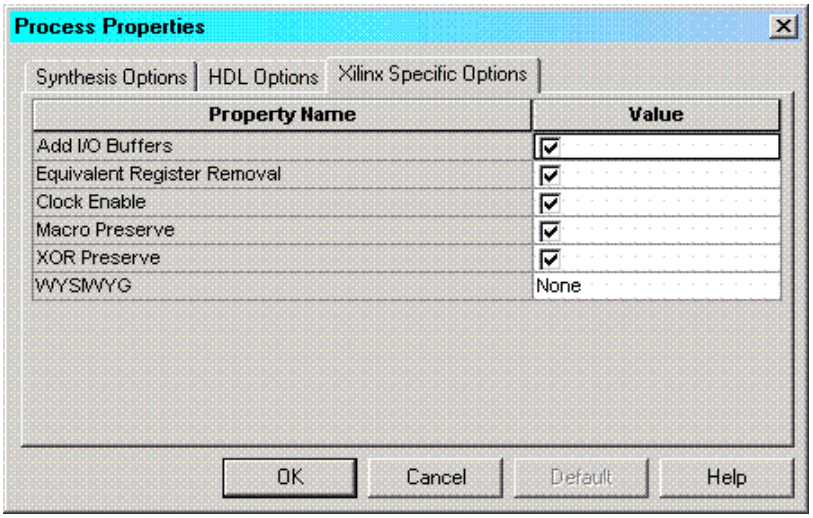


Figure 3-9: **Xilinx Specific Options (CPLDs)**

Following is a list of the Xilinx Specific Options:

- Equivalent Register Removal
  See "EQUIVALENT_REGISTER_REMOVAL".
- Max Fanout (FPGA Only)
  See "MAX_FANOUT".
- Number of Clock Buffers (FPGA Only)
  See "BUFG (CPLD)".
- Register Balancing (FPGA Only)
  See "REGISTER_BALANCING".

- Move First Flip-Flop Stage (FPGA Only)
  See "MOVE_FIRST_STAGE".
- Move Last Flip-Flop Stage (FPGA Only)
  See "MOVE_LAST_STAGE".
- Slice Packing (FPGA Only)
- Pack I/O Registers into IOBs (FPGA Only)
  See "IOB".

Setting Implementation Options

For FPGAs, the implementation process properties specify how a design is translated, mapped, placed, and routed. You can set multiple properties to control the implementation processes for the design. For CPLDs, they control how a design is translated and fit.

See the online help for the Process Properties dialog box for details.

Floorplanner

The following sections explain how to set area and IOB constraints using the Floorplanner.

For a list of supported constraints, see "Constraint Entry Table".

Using Area Constraints

Area constraints are a way of restricting where PAR can place a particular piece of logic. By reducing PAR's search area for placing logic, PAR's performance may be improved.

To create an area constraint, do the following steps.

1. From within the Floorplanner, select a hierarchical group in the Design Hierarchy window.
2. Select **Floorplan** → **Assign Area Constraint**.
3. In the Floorplan window, use the mouse to drag out a rectangular box where you want the area constraint to be located. The area constraint will cover all the tiles that are inside the drag box.

Area constraints may overlap each other. Select **Floorplan** → **Bring Area To Front** or **Floorplan** → **Push Area To Back** to move a selected area constraint in front of or behind another.

Creating UCF Constraints from IOB Placement

You can also add constraints to the UCF file through the Floorplanner and iteratively implement your design to achieve optimal placement.

To begin with, you need only the NGD file generated in a previous flow. In the Floorplanner, you manually make IOB assignments which are automatically written into the UCF file. The Floorplanner edits the UCF file by adding the newly created placement constraints. The placement constraints you create in the Floorplanner take precedence over existing constraints in the UCF.

Next, go through the steps of implementing your design by running NGDBuild, MAP, and PAR.

PACE

You can set constraints in PACE (Pinout & Area Constraints Editor).

Within PACE, the Pin Assignments Editor is mainly used for assigning location constraints to IOs in designs. It is also used to assign certain IO properties like IO Standards.

- LOC constraints for IOs (including Bank and Edge constraints) and global logic, for example
  - IOs

    NET “*name*” LOC = "A23";

    NET “*name*” LOC = "BANK0";

    NET “*name*” LOC = "TL"; `//half-edge constraint`

    NET “*name*” LOC = "T"; `//edge constraint`
  - Global Logic

    INST “*gt_name*” LOC = GT_X0Y0;

    INST “*bram_name*” LOC = RAMB16_X0Y0; `(or RAMB4_C0R0)`

    INST “*dcm_name*” LOC = DCM_X0Y0;

    INST “*ppc_name*” LOC = PPC405_X0Y0;

    INST “*mult_name*” LOC = MULT18X18_X0Y0;
- IOSTANDARD constraints

  NET “*name*” IOSTANDARD = "LVTTL";
- PROHIBIT constraints

  CONFIG PROHIBIT = A23;

  CONFIG PROHIBIT = SLICE_X1Y6;

  CONFIG PROHIBIT = TBUF_X0Y0; (RAMs, MULTs, GTs, DCMs also)

The AREA Constraints Editor is mainly used to assign areas to hierarchical blocks of logic. The following UCF examples show AREA_GROUP constraints that can be set in the AREA Constraints Editor.

INST “*name*” AREA_GROUP = *group_name*;

AREA_GROUP “*group_name*” RANGE=SLICE_X1Y1:SLICE_X5Y5;

AREA_GROUP “*group_name*” RANGE = SLICE_X6Y6:SLICE_X10Y10, SLICE_X1Y1:SLICE_X4Y4;

AREA_GROUP “*group_name*” COMPRESSION = 0;

AREA_GROUP “*group_name*” ROUTE_AREA = FIXED;

Note: SLICE_ would be CLB_ for Virtex, Virtex-E, Spartan-II, and Spartan-IIE.

You can access PACE from the Processes window in the Project Navigator. Double-click Assign Package Pins or Create Area Constraints under User Constraints.

For details on how to use PACE, see the PACE online help, especially the topics within Editing Pins and Areas in the Procedures section.

FPGA Editor

You can add certain constraints to or delete certain constraints from the PCF file in the FPGA Editor. In the FPGA Editor, net, site, and component constraints are supported as property fields in the individual nets and components. Properties are set with the Setattr command and are read with the Getattr command. All Boolean constraints (block, locate,

lock, offset, and prohibit) have values of On or Off; offset direction has a value of either In or Out; and offset order has a value of either Before or After. All other constraints have a numeric value and can also be set to Off to delete the constraint. All values are case-insensitive (for example, “On” and “on” are both accepted).

When you create a constraint in the FPGA Editor, the constraint is written to the PCF file whenever you save your design. When you use the FPGA Editor to delete a constraint and then save your design file, the line on which the constraint appears in the PCF file remains in the file but it is automatically commented out.

Some of the constraints supported in the FPGA Editor are listed in the following table.

Table 3-1: **Constraints**

Constraint	Accessed Through
block paths	Component Properties and Path Properties property sheet
define path	Viewed with Path Properties property sheet
location range	Component Properties Constraints page
locate macro	Macro Properties Constraints page
lock placement	Component Properties Constraints page
lock routing of this net	Net Properties Constraints page
lock routing	Net Properties Constraints page
maxdelay allnets	Main Properties Constraints page
maxdelay allpaths	Main Properties Constraints page
maxdelay net	Net Properties Constraints page
maxdelay path	Path Properties property sheet
maxskew	Main Properties Constraints page
maxskew net	Net Properties Constraints page
offset comp	Component Properties Offset page
penalize tilde	Main Properties Constraints page
period	Main Properties Constraints page
period net	Net Properties Constraints page
prioritize net	Net Properties Constraints page
prohibit site	Site Properties property sheet

Locked Nets and Components

If a net is locked, you cannot unroute any portion of the net, including the entire net, a net segment, a pin, or a wire. To unroute the net, you must first unlock it. You can add pins or routing to a locked net.

A net is displayed as locked in the FPGA Editor if the Lock Net [*net_name*] constraint is enabled in the PCF file. You can use the Net Properties property sheet to remove the lock constraint.

When a component is locked, one of the following constraints is set in the PCF file.

```
lock comp [comp_name]
locate comp [comp_name]
lock macro [macro_name]
lock placement
```

If a component is locked, you cannot unplace it, but you can unroute it. To unplace the component, you must first unlock it.

Interaction Between Constraints

Schematic constraints are placed at the beginning of the PCF file by MAP. The start and end of this section is indicated with **SCHEMATIC START** and **SCHEMATIC END**, respectively. Because of a "last-read" order, all constraints that you enter in this file should come after **SCHEMATIC END**.

You are not prohibited from entering a user constraint before the schematic constraints section, but if you do, a conflicting constraint in the schematic-based section may override your entry.

Every time a design is remapped, the schematic section of the PCF file is overwritten by the mapper. The user constraints section is left intact, but certain constraints may be invalid because of the new mapping.

Constraints Priority

In some cases, two timing specifications cover the same path. For cases where the two timing specifications on the path are mutually exclusive, the following constraint rules apply.

- Priority depends on the file in which the constraint appears. A constraint in a file accessed later in the design flow replaces a constraint in a file accessed earlier in the design flow (Last One Wins) if the constraint name is the same in both files. If the two constraints have different names, the last one in the PCF file has priority.

  Priority is as follows (first listed is the highest priority, last listed is the lowest).

  - Constraints in a Physical Constraints File (PCF) -- Highest Priority
  - Constraints in a User Constraints File (UCF)
  - Constraints in a Netlist Constraints File (NCF)
  - Attributes in a schematic -- Lowest Priority
- If two timing specifications cover the same path, the priority is as follows (first listed is the highest priority, last listed is the lowest).
  - Timing Ignore (TIG)
  - FROM THRU TO
  - FROM TO
  - Specific OFFSET

- Group OFFSET
- Global OFFSET
- PERIOD

- FROM THRU TO or FROM TO statements have a priority order that depends on the type of source and destination groups included in a statement. The priority is as follows (first listed is the highest priority, last listed is the lowest).
  - Both the source group and the destination group are user-defined groups
  - Either the source group or the destination group is a predefined group
  - Both the source group and the destination group are predefined groups
- OFFSET constraints take precedence over more global constraints.

  If two specific OFFSET constraints at the same level of precedence interact, an OFFSET with a register qualifier takes precedence over an OFFSET without a qualifier; if otherwise equivalent, the latter in the constraint file takes precedence.
- Net delay and net skew specifications are analyzed independently of path delay analysis and do not interfere with one another.

There are circumstances in which constraints priority may not operate as expected. These cases include supersets, subsets, and intersecting sets of constraints. See the following diagram.

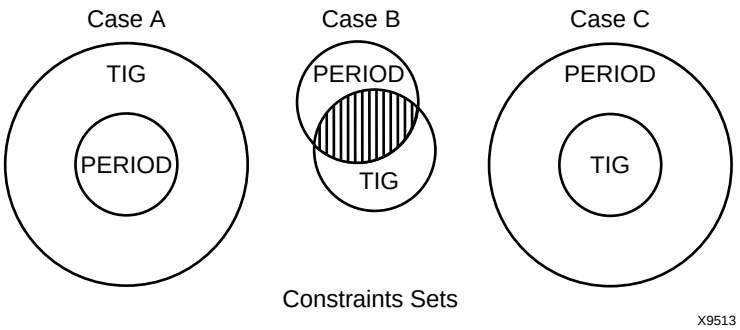


Figure 3-10: **Interaction Between Constraints Sets**

In Case A, the TIG superset will create issues with the PERIOD set. In Case B, the intersection of the PERIOD and TIG sets creates an ambiguous circumstance where constraints may sometimes be considered as part of TIG and at other times part of PERIOD. In Case C, the TIG subset will work normally within the PERIOD superset.

Constraint Entry Table

The table below shows whether a constraint can be entered using a particular method. For detailed information about a specific constraint, click its name in the Constraints column.

Table 3-2: **Constraints Entry Table**

Constraint	Schematic	VHDL	Verilog	ABEL	NCF	UCF	Xilinx CE	PCF	XCF	Floorplanner	PACE	FPGA Editor	XST Cmd Line	Proj. Nav.
Note: (1) Use cautiously. Although the constraint is available, there are differences between the UCF/NCF and PCF syntax. (2) Not recommended. (3) Pin assignments are specified in ABEL PIN declarations without using the LOC keyword. (4) Specified using ABEL-specific keyword 'RETAIN'.														
Constraints A														
AREA_GROUP	√				√	√				√	√			
ASYNC_REG		√	√		√	√	√							
Constraints B														
BEL	√	√	√		√	√								
BLKNM	√	√	√		√	√			√					
BOX_TYPE		√	√						√					
BRAM_MAP	√	√	√			√							√	
BUFFER_TYPE		√	√						√					
BUFG (CPLD)	√	√	√	√	√	√			√					
BUFGCE		√	√						√					
Constraints C														
CLK_FEEDBACK	√	√	√		√	√								
CLKDV_DIVIDE	√	√	√		√	√			√					
CLKFX_DIVIDE	√	√	√		√	√						√		
CLKFX_MULTIPLY	√	√	√		√	√						√		
CLKIN_DIVIDE_BY_2	√	√	√			√								
CLKIN_PERIOD	√	√	√			√						√		
CLKOUT_PHASE_SHIFT	√	√	√		√	√								
CLOCK_BUFFER		√	√						√					
CLOCK_SIGNAL		√	√						√					
COLLAPSE	√	√	√		√	√								
COMPGRP								√						
CONFIG					√	√								√

Table 3-2: **Constraints Entry Table**

Constraint	Schematic	VHDL	Verilog	ABEL	NCF	UCF	Xilinx CE	PCF	XCF	Floorplanner	PACE	FPGA Editor	XST Cmd Line	Proj. Nav.
Note: (1) Use cautiously. Although the constraint is available, there are differences between the UCF/NCF and PCF syntax. (2) Not recommended. (3) Pin assignments are specified in ABEL PIN declarations without using the LOC keyword. (4) Specified using ABEL-specific keyword 'RETAIN'.														
CONFIG_MODE						√								
COOL_CLK	√	√	√	√	√	√								
Constraints D														
DATA_GATE	√	√	√	√	√	√								
DCI_VALUE					√	√								
DECODER_EXTRACT		√	√						√				√	√
DESKEW_ADJUST		√	√			√								
DFS_FREQUENCY_MODE	√	√	√		√	√								
Directed Routing					√	√						√		
DISABLE					√	√		√						
DLL_FREQUENCY_MODE	√	√	√		√	√								
DRIVE	√	√	√		√	√	√		√					
DROP_SPEC					√	√		√ (1)						
DUTY_CYCLE_CORRECTION	√	√	√		√	√			√					
Constraints E														
ENABLE					√	√		√						
ENUM_ENCODING		√							√					
EQUIVALENT_REGISTER_REMOVAL		√	√						√				√	√
Constraints F														
FAST	√	√	√	√	√	√	√		√					
FEEDBACK						√		√	√					
FILE	√													
FLOAT	√	√	√	√	√	√			√					
FROM-THRU-TO					√	√	√	√						
FROM-TO					√	√	√	√						
FSM_ENCODING		√	√						√				√	√

Table 3-2: **Constraints Entry Table**

Constraint	Schematic	VHDL	Verilog	ABEL	NCF	UCF	Xilinx CE	PCF	XCF	Floorplanner	PACE	FPGA Editor	XST Cmd Line	Proj. Nav.
Note: (1) Use cautiously. Although the constraint is available, there are differences between the UCF/NCF and PCF syntax. (2) Not recommended. (3) Pin assignments are specified in ABEL PIN declarations without using the LOC keyword. (4) Specified using ABEL-specific keyword 'RETAIN'.														
FSM_EXTRACT		√	√						√				√	√
FSM_STYLE		√	√		√	√			√					
FULL_CASE			√										√	√
Constraints H														
HBLKNM	√	√	√		√	√								
HIGH_FREQUENCY	√	√	√		√	√								
HU_SET	√	√	√		√	√			√					
Constraints I														
INCREMENTAL_SYNTHESIS		√	√						√					
INIT	√	√	√	√	√	√#	√					√		
#INIT is not supported in the UCF for some memory elements. An error will occur in these cases indicating that the constraint should be applied to the NCF or netlist.														
INIT_A	√	√	√		√	√								
INIT_B	√	√	√		√	√								
INIT_xx	√	√	√		√	√			√					
INITP_xx	√	√	√			√								
INREG	√			√		√								
IOB	√	√	√		√	√	√		√				√	√
IOBDELAY	√	√	√		√	√	√							
IOSTANDARD	√	√	√	√	√	√	√		√		√			
Constraints K														
KEEP	√	√	√	√	√	√			√					
KEEP_HIERARCHY	√	√	√		√	√			√				√	√
KEEPER	√	√	√	√	√	√	√		√					
Constraints L														
LOC	√	√	√	√ (3)	√	√	√	√ (1)	√	√	√			
LOCATE								√				√		

Table 3-2: **Constraints Entry Table**

Constraint	Schematic	VHDL	Verilog	ABEL	NCF	UCF	Xilinx CE	PCF	XCF	Floorplanner	PACE	FPGA Editor	XST Cmd Line	Proj. Nav.
Note: (1) Use cautiously. Although the constraint is available, there are differences between the UCF/NCF and PCF syntax. (2) Not recommended. (3) Pin assignments are specified in ABEL PIN declarations without using the LOC keyword. (4) Specified using ABEL-specific keyword 'RETAIN'.														
LOCK								√				√		
LOCK_PINS		√			√	√								
LUT_MAP		√	√						√					
Constraints M														
MAP	√				√	√								
MAX_FANOUT		√	√						√				√	√
MAXPT		√	√	√	√	√								
MAXSKEW	√	√	√		√	√		√ (1)				√		
MOVE_FIRST_STAGE		√	√						√				√	√
MOVE_LAST_STAGE		√	√						√				√	√
MULT_STYLE		√	√						√				√	√
MUX_EXTRACT		√	√						√				√	√
MUX_STYLE		√	√						√				√	√
Constraints														
NODELAY	√	√	√		√	√			√					
NOREDUCE	√	√	√	√(4)	√	√			√					
Constraints O														
OFFSET	√				√	√	√	√ (1)	√					
ONESHOT	√	√	√											√
OPEN_DRAIN	√	√	√	√	√	√			√					
OPT_EFFORT	√				√	√								√
OPT_LEVEL		√	√						√				√	√
OPT_MODE		√	√						√				√	√
OPTIMIZE	√		√		√	√								√
OPTIMIZE_PRIMITIVES	√	√	√		√	√			√					

Table 3-2: **Constraints Entry Table**

Constraint	Schematic	VHDL	Verilog	ABEL	NCF	UCF	Xilinx CE	PCF	XCF	Floorplanner	PACE	FPGA Editor	XST Cmd Line	Proj. Nav.
Note: (1) Use cautiously. Although the constraint is available, there are differences between the UCF/NCF and PCF syntax. (2) Not recommended. (3) Pin assignments are specified in ABEL PIN declarations without using the LOC keyword. (4) Specified using ABEL-specific keyword 'RETAIN'.														
Constraints P														
PARALLEL_CASE			√										√	√
PERIOD	√	√	√		√	√	√	√ (1)	√			√		
PHASE_SHIFT	√	√	√		√	√						√		
PIN						√								
PRIORITY					√	√		√						
PRIORITY_EXTRACT		√	√						√				√	√
PROHIBIT		√	√		√	√	√	√ (1)		√	√	√		
PULLDOWN	√	√	√		√	√	√		√					
PULLUP	√	√	√	√	√	√	√		√					
PWR_MODE	√	√	√	√	√	√			√					
Constraints R														
RAM_EXTRACT		√	√						√				√	√
RAM_STYLE		√	√						√				√	√
REG	√	√	√	√	√	√			√					
REGISTER_BALANCING		√	√						√				√	√
REGISTER_DUPLICATION		√	√						√					√
REGISTER_POWERUP		√							√				√	
RESOURCE_SHARING		√	√						√				√	√
RESYNTHESIZE		√	√						√					
RLOC	√	√	√		√	√			√	√				
RLOC_ORIGIN	√	√	√		√	√		√		√				
RLOC_RANGE	√	√	√		√	√		√	√					
ROM_EXTRACT		√	√						√				√	√
ROM_STYLE		√	√						√				√	√

Table 3-2: **Constraints Entry Table**

Constraint	Schematic	VHDL	Verilog	ABEL	NCF	UCF	Xilinx CE	PCF	XCF	Floorplanner	PACE	FPGA Editor	XST Cmd Line	Proj. Nav.
Note: (1) Use cautiously. Although the constraint is available, there are differences between the UCF/NCF and PCF syntax. (2) Not recommended. (3) Pin assignments are specified in ABEL PIN declarations without using the LOC keyword. (4) Specified using ABEL-specific keyword 'RETAIN'.														
Constraints S														
SAVE NET FLAG	√	√	√		√	√			√					
SCHMITT_TRIGGER	√	√	√	√	√	√			√					
SHIFT_EXTRACT		√	√						√				√	√
SHREG_EXTRACT		√	√						√				√	√
SIGNAL_ENCODING		√	√						√				√	
SLEW	√	√	√		√	√	√		√					
SLICE_PACKING													√	√
SLICE_UTILIZATION_RATIO		√	√						√				√	√
SLICE_UTILIZATION_RATIO_MAXMARGIN		√	√						√				√	
SLOW	√	√	√	√	√	√	√		√					
SRVAL	√	√	√		√	√								
SRVAL_A	√	√	√		√	√								
SRVAL_B	√	√	√		√	√								
STARTUP_WAIT	√	√	√		√	√			√					
SYSTEM_JITTER	√	√	√		√	√			√					
Constraints T														
TEMPERATURE					√	√	√	√						
TIG	√	√	√		√	√	√	√ (1)	√					
TIMEGRP						√	√	√	√					
TIMESPEC					√	√	√							
TNM	√			√	√	√	√							
TNM_NET	√				√	√	√							
TPSYNC	√				√	√								
TPTHRU	√				√	√	√							

Table 3-2: **Constraints Entry Table**

Constraint	Schematic	VHDL	Verilog	ABEL	NCF	UCF	Xilinx CE	PCF	XCF	Floorplanner	PACE	FPGA Editor	XST Cmd Line	Proj. Nav.
Note: (1) Use cautiously. Although the constraint is available, there are differences between the UCF/NCF and PCF syntax. (2) Not recommended. (3) Pin assignments are specified in ABEL PIN declarations without using the LOC keyword. (4) Specified using ABEL-specific keyword 'RETAIN'.														
TRANSLATE_OFF and TRANSLATE_ON		√	√											
TSidentifier					√	√	√	√ (1)				√		
Constraints U														
U_SET	√	√	√		√	√			√					
USE_CARRY_CHAIN	√	√	√						√				√	
USE_RLOC	√	√	√		√	√			√					
USELOWSKEWLINES	√	√	√		√	√	√	√	√					
Constraints V														
VOLTAGE					√	√	√	√						
VREF	√				√	√								
Constraints W														
WIREAND	√	√	√		√	√								
WRITE_MODE	√	√	√		√	√								
WRITE_MODE_A	√	√	√		√	√								
WRITE_MODE_B	√	√	√		√	√								
Constraints X														
XBLKNM	√	√	√		√	√			√					
XOR_COLLAPSE		√	√						√				√	√

Chapter 4

Timing Constraint Strategies

This chapter contains the following sections:

FPGA Timing Constraint Strategies

This section provides general guidelines that explain how to constrain the timing on designs when using the implementation tools for FPGAs.

For more information about timing constraints and strategies, go to the Xilinx home page, click Support. Then select **Tech Tips** → **Timing & Constraints**.

Basic Implementation Tools Constraining Methodology

Creating global constraints for a design is the easiest way to provide coverage of the constrainable connections in a design and guide the tools to meet timing requirements for all paths. The global constraints constrain the whole design. If there are multi-cycle or static paths, you can constrain them using more specific constraints. A multi-cycle path is a path between two registers with a timing requirement that is a multiple of the clock period for the registers. A static path does not include clocked elements, for example, pad-to-pad paths.

Xilinx recommends specifying the exact value required for a path as opposed to over-tightening a specification. Specifying tighter constraints than required is not recommended because tighter constraints can lengthen PAR runtimes and cause degradation in the quality of results.

The Constraints Editor is designed around the methodology discussed in this chapter. The group names and TSids in the examples show how the Constraints Editor populates the grids and creates new groups and constraints. The Constraints Editor provides additional help; the clocks and IOs are supplied so you do not have to come up with the exact spelling of the names and only have to define the timing and not the syntax of the constraints. For more specific grouping, element names are provided, and exceptions to the global constraints can be made using those groups.

The first tab of the Constraints Editor shows all the global paths that need to be covered. If this tab is completed, all synchronous paths will be covered.

Note: All examples in this chapter show the UCF syntax.

Global Timing Assignments

Global timing assignments are overall constraints that cover all constrainable paths in a design. These assignments include clock definitions, input and output timing requirements, and combinatorial path requirements.

Following are some recommendations for assigning definitions.

Assigning Definitions for Clocks Driven by Pads

Define each clock in the design. Defining each clock covers all synchronous paths within each clock domain and paths that cross between related clock domains. Use a TNM_NET on each clock net (on the net attached to the pad, usually the port name in HDL) and then use the TIMESPEC PERIOD syntax with the TNM_NET group created. Using the TIMESPEC version of the PERIOD definition allows for greater path control later on when constraining paths between clock domains.

See "Assigning Definitions for DLL / DCM Clocks" if using a Virtex DLL / DCM.

Related Clocks Example

The following example design has two clocks. TNM_NETs identify the synchronous elements of each clock domain. TIMESPEC PERIOD gives the flexibility to describe inter clock domain path requirements. The clock, "clock2_in," has twice the period of "clock1_in" which is shown in the following UCF example with the clock2_in PERIOD definition using a function of the "TS_clock1_in" specification ("TS_clock1_in" * 2).

```
NET "clock1_in" TNM_NET =  "clock1_in";
TIMESPEC "TS_clock1_in" = PERIOD "clock1_in" 20 ns HIGH 10;
NET "clock2_in" TNM_NET = "clock2_in";
TIMESPEC "TS_clock2_in" = PERIOD "clock2_in" "TS_clock1_in" * 2;
```

The Constraints Editor uses the clock pad net name for the group name and the TSid as show in the previous example. This feature is important if you want to override a constraint that was entered in the source.

PHASE Related Clocks Example

The following example shows how to specify two clocks related by a phase difference. The clock "clock" has a period of 10ns, "clock_90" is also 10 ns, but is shifted 90 degrees out of phase or is lagging "clock's" rising edge by 2.5 ns. You can use the keyword "PHASE" that allows you to identify this relationship. The timing tools use this information in OFFSET and cross-clock domain paths. See the following example.

```
NET "clock" TNM_NET = "clock";
TIMESPEC "TS_clock" = PERIOD "clock" 10 ns HIGH 50%;
NET "clock_90" TNM_NET = "clock_90";
TIMESPEC "TS_clock_90" = PERIOD "clock_90" "TS_clock" * 1 PHASE + 2.5ns;
```

Assigning Definitions for DLL/DCM Clocks

TRANSLATION (NGDBuild) propagates TNM_NET tags through DLLs and DCMs. NGDBuild creates new TNM_NETs for each of the DLL and DCM output taps and associated PERIOD statements. The code takes into account the phase relationship factor of the outputs for the DLL, and also performs the appropriate multiplication or division of the PERIOD value.

The code also takes into account any of the PHASE taps adjustments. This means that for OFFSETs and cross-clock domain paths, the timing tools now know the relationship for PHASE shifts also.

DCM PERIOD Propagation Example

In this example, you only need to define the input clock to the DCM and the tools will generate all of the correct PERIODs for the output taps. Assume that the input clock (net "clock_in" with PERIOD 30 ns) DCM in this example uses the CLK0 (net "clock0") and CLK2X180 (net "clock2x180") output taps. When you define the input clock, the system performs all of the transformations.

For input clock “clock_in”:

```
NET "clock_in" TNM_NET = "clock_in";
TIMESPEC "TS_clock_in" = PERIOD "clock_in" 30 ns HIGH 50%;
```

Generated clock definitions:

```
NET "clock0" TNM_NET = "clock0";
TIMESPEC "TS_clock0" = PERIOD "TS_clock_in" * 1;
NET "clock2x180" TNM_NET = "clock2x180";
TIMESPEC "TS_clock2x180" = PERIOD "TS_clock_in" / 2 PHASE + 7.50 ns;
```

Assigning Definitions for Derived and Gated Clocks

For clocks that are created in the FPGA, such as the output of a register or a gated clock (the output of combinatorial logic), the net name from the output of the register or gate should be the name used for the TNM_NET group name and TS*id*.

See “OFFSETs with Derived or Gated Clocks”.

Assigning Input and Output Requirements

Constrain input and output timing requirements using the OFFSET constraints. Pad to Setup requirements use OFFSET IN BEFORE and for Clock to Out requirements use OFFSET OUT AFTER. You can specify OFFSETs in three levels of coverage.

- The first, global OFFSET applies to all inputs or outputs for a specific clock.
- The second, a group OFFSET form, identifies a group of inputs or outputs clocked by a common clock that have the same timing requirements.
- The third, a specific OFFSET form, specifies the timing by each input or output.

OFFSET constraints of a more specific scope override a more general scope.

A group OFFSET overrides a global OFFSET specified for the same IOs. A specific OFFSET overrides both global and group OFFSETs if used. This priority rule allows you to start with global OFFSETs, then create group or specific OFFSETs for IOs with special timing requirements.

For memory usage and runtime considerations, use global and group OFFSETs and avoid specific OFFSETs whenever possible. Using wildcards in the specific OFFSET form creates multiple specific OFFSET constraints, not a group OFFSET.

Example:

```
NET bob* OFFSET = IN 5 AFTER clock;
```

Global Inputs Requirements

Use OFFSET IN BEFORE to define Pad to Setup timing requirements. OFFSET IN BEFORE is an external clock-to-data relationship specification and takes into account the clock delay, clock edge and DLL / DCM introduced clock phase when analyzing the setup requirements (data delay + setup - clock delay-clock arrival).). Clock arrival takes into account any clock phase generated by the DLL / DCM or clock edge. This strategy constrains all of the inputs clocked by the same clock to identical requirements.

Following is a global OFFSET IN BEFORE example:

```
OFFSET = IN value units BEFORE clock_pad_net;
OFFSET = IN 10 ns BEFORE “clock_in”;
```

where

- *value* is the time allowed for the data to propagate from the pad to meet a setup requirement to the clock. This value is in relationship to the clocks initial edge at the pin of the chip. (The PERIOD constraint defines the clock initial edge.)
- *units* is ms, us, ns (default) or ps
- *clock_pad_net* is the name of the clock using the net name attached to the pad (This or the port name for HDL designs).

Global Outputs Requirements

Use OFFSET OUT AFTER to define Clock to Pad timing requirements. OFFSET OUT AFTER is an external clock-to-data specification and takes into account the clock delay, clock edge and DLL / DCM introduced clock phase when analyzing the setup requirements (clock delay + clock to out + data delay +clock arrival). Clock arrival takes into account any clock phase generated by the DLL / DCM or clock edge. This strategy constrains all of the outputs clocked by the same clock to the same requirement.

The following is a global OFFSET OUT AFTER example:

```
OFFSET = OUT value units AFTER clock_pad_net;
OFFSET = OUT 10 ns AFTER "clock_in";
```

where

- *value* is the time allowed for the data to propagate from the synchronous element (clock to out, T_{CKO}) to the pad. This value is in relationship to the clocks initial edge at the pin of the chip. (The PERIOD constraint defines the clock initial edge.)
- *units* is ms, us, ns (default) or ps
- *clock_pad_net* is the name of the clock using the net name attached to the pad or the port name for HDL designs.

Assigning Global Pad to Pad Requirements

Use a FROM PADS TO PADS constraint to globally constrain all combinatorial pin-to-pin paths. If you do not have any combinatorial pin-to-pin paths, ignore this constraint.

Following a global pad to pad example:

```
TIMESPEC “TSid” = FROM “PADS” TO “PADS” value units;
TIMESPEC “TS_P2P” = FROM “PADS” TO “PADS” 10 ns;
```

where

- *id* is a user-specified unique identifier for the constraint
- *value* is the time allowed for the data to propagate from an input pad to an output pad
- *units* is ms, us, ns (default) or ps

Specific Timing Assignments

If there are paths that are static in nature, you can use TIG to eliminate the paths from timing consideration in Place and Route (PAR) and TRCE. If there are paths that require faster or slower specifications than the global requirements, you can create fast or slow exceptions for those paths. If multi-cycle paths exist, identify and constrain them.

Note: The tigs paths still show the longest delay for that constraint in the verbose timing report. Net tigs can be turned off in the Timing Analyzer to see the actual timing on these nets.

Ignored Paths (TIG)

You can specify false paths (paths to ignore) in two different ways—by nets and elements or by timing paths. Identifying false paths allows PAR to concentrate on more critical paths when placing components and when using routing resources. There might be less runtime because PAR does not have to meet a specific timing requirement. Creating a large number of path tigs can increase memory usage and possibly increase runtime due to the extra paths models that are created.

By Nets or Elements

These paths are ignored by both PAR and timing analysis and do not show up in the timing report. Also these paths are not included in the Connection Coverage statistic. See "Ignored Paths (TIG)" for more information.

- False Paths by Net

  You can define false paths for *all* paths that pass through a particular net using the following UCF syntax:

  ```
  NET "net_name" TIG;
  ```

  You can also define false paths for a specified set of paths that pass through a particular net using the following UCF syntax:

  ```
  NET "net_name" TIG = TSid_list;
  ```

  where

  - *net_name* is the name of the net that the paths are passing through.
  - TS*id_list* is a comma-delimited list of TIMESPEC identifiers to which the TIG applies.

- False Paths by Instance

  You can define false paths for *all* paths that pass through a particular instance using the following UCF syntax:

  ```
  INST "inst_name" TIG;
  ```

  You can also define false paths for a specified set of paths that pass through a particular instance using the following UCF syntax:

  ```
  INST "inst_name" TIG = TSid_list;
  ```

where

- *inst_name* is the name of the instance that the paths are passing through
- TS*id_list* is a comma-delimited list of TIMESPEC identifiers to which the TIG should apply

- False Paths by Pin

  You can define false paths for *all* paths that pass through a particular instance pin using the following UCF syntax:

  ```
  PIN "instance.pin_name" TIG;
  ```

  You can also define false paths for a specified set of paths that pass through a particular instance pin using the following UCF syntax:

  ```
  PIN "instance.pin_name" TIG = TSid_list;
  ```

  where

  - *instance.pin_name* is the name of the instance and the pin identifier separated by a period that the paths are passing through
  - TS*id_list* is a comma-delimited list of TIMESPEC identifiers to which the TIG should apply

False Paths by Timing Path

You can create groups, use the FROM TO, FROM THRU TO, or open FROM or TO constraints, and then specify TIG as the path value. See "False Paths by Path" for syntax usage. These paths show up in a timing analysis report, but the timing is not considered. These paths are also included in the connection coverage statistics.

Following is a FROM TO TIG example:

```
TIMESPEC "TSid" = FROM "from_grp" TO "to_grp" TIG;
```

where

- *id* is a user-specified unique identifier for the constraint
- *from_grp* and *to_grp* are TIMEGRPs

Following is a FROM THRU TO TIG example:

```
TIMESPEC "TSid" = FROM "from_grp" THRU "thru_pt" TO "to_grp" TIG;
```

where

- *id* is a user-specified unique identifier for the constraint
- *from_grp* and *to_grp* are TIMEGRPs
- *thru_pt* is a net, instance or pin

See "TPTHRU" for details on defining TPTHRU points.

Asynchronous Set/Reset Paths

The tools do not automatically analyze asynchronous set/reset paths. Automatic analysis is controlled by the path tracing controls. See "DISABLE" and "ENABLE".

Multi-Cycle and Fast or Slow Timing Assignments

These path assignments include multi-cycle paths and fast or slow exceptions. First create timing groups to define start point and end points for the paths. These groups are used in the FROM TO timing constraints to override the PERIOD constraints for these specific paths. The following sections describe different exception types.

Cross-Clock Domain Constraining

The timing tools no longer include domain paths in the destination register clock domain if the clocks are not defined as related. Related clock domains are defined in the system as a function of other clock TIMESPECs. The TRANSLATE (NGDBuild) phase automatically relates clocks from the outputs of a DLL / DCM. If the paths between two "related" clocks are false or require a different time requirement than calculated, then create a FROM:TO constraint with a TIG or the correct value. If the clocks are unrelated but have valid paths between them, then create FROM TO constraints to constrain them. To constrain paths between two clocks and use the groups created by each clock domain, create a FROM TO for each direction that paths pass between the two clock domains, then specify the time requirement according to the path requirement. See "Related Clocks Example" to see how the groups were created.

Following is a cross-clock domain TIMESPEC example:

```
TIMESPEC "TS_clock1_in_2_clock2_in" = FROM "clock1_in" TO "clock2_in"
10 ns;
```

User Group Creation

You can create groups to identify path end points. There are three basic methods allowed for creating groups.

- By connectivity
- By hierarchy
- By elements

The types of elements that can be grouped are FFS, PADS, RAMS, BRAMS_PORTA, BRAMS_PORTB, CPUS, MULTS, HSIOS and LATCHES. These are considered reserved keywords that define the types of synchronous elements in FPGAs and pads.

There are four different basic ways to create user groups.

- Identifying Groups by Connectivity

  Identifying groups by connectivity allows you to group elements by specifying nets that eventually drive synchronous elements and pads. This method is a good way to identify multi-cycle paths elements that are controlled by a clock enable. This method uses TNM_NET on a net.

  The TNM_NET syntax for identifying groups by connectivity is:

  ```
  NET "net_name" TNM_NET = qualifier "tnm_name";
  ```

  where

  - *net_name* is the name of a net propagated by the tools to the element ends.
  - *tnm_name* is the user-assigned name for the group created by the TNM_NET. Multiple nets can be assigned the same *tnm_name*.
  - An optional *qualifier* of FFS, PADS, RAMS, BRAMS_PORTA, BRAMS_PORTB, CPUS, MULTS, HSIOS or LATCHES may be used when the *net_name* contains wildcards.

- Identifying Groups by Hierarchy

  Identifying groups by hierarchy allows you to group by traversing the hierarchy of a module and tagging all predefined elements with the TNM. This method uses a TNM on a block. The TNM syntax for identifying groups by hierarchy is:

  INST "*inst_name*" **TNM =** *qualifier* "*tnm_name*";

  where

  - *inst_name* is the hierarchical name of a macro or module to be traversed by the tools to identify underlying elements for the group labeled by the *tnm_name* label.
  - An optional *qualifier* of FFS, PADS, RAMS, BRAMS_PORTA, BRAMS_PORTB, CPUS, MULTS, HSIOS or LATCHES may be used.

- Identifying Specific Elements by Instance Name

  Identifying elements directly allows you to group by tagging predefined elements with a TNM. Multiple instances can be given the same *tnm_name*.

  The TNM syntax for identifying groups by instance is:

  INST "*inst_name*" **TNM =** *qualifier* "*tnm_name*";

  where

  - *inst_name* is the predefined instance name for the group labeled by the *tnm_name* label.
  - An optional *qualifier* of FFS, PADS, RAMS, BRAMS_PORTA, BRAMS_PORTB, CPUS, MULTS, HSIOS or LATCHES may be used when the *inst_name* contains wildcards.

- Identifying Elements for Groups using Element Output Net Names

  This method is mainly used by schematic users who generally name nets, not instances. Identifying elements individually is used for singling out elements or identifying elements by output net name. This method uses TIMEGRP and allows the use of wildcards (*, ?) for filtering elements. This method is best used for schematics where the instance names are rarely known but the output nets generally are.

  The TIMEGRP syntax for identifying groups by element output net name is:

  TIMEGRP "*tgrp_name*" **=** *qualifier* (*output_net_name*);

where

- *tgrp_name* is the name assigned by you to the group
- *qualifier* is a (FFS, PADS, RAMS, BRAMS_PORTA, BRAMS_PORTB, CPUS, MULTS, HSIOS, LATCHES) keyword
- *output_net_name* is the output net name for each element that you would like to group. You can use wildcards with *output_net_name*.

Specific OFFSET Constraints Using PAD and or Register Groups

You can use grouping with OFFSET. Grouping includes both register groups and pad groups. Grouping allows you to group pads to set the same path delay requirements and group registers for identifying paths that have different requirements from or to single pads. You can group and constrain the single pads and registers all at once. This is useful if a clock is used on the rising and falling edge for inputs or outputs. These two groups will require different constraints.

- Group OFFSET IN Example

  TIMEGRP “*pad_group*” **OFFSET = IN** *time units* **BEFORE** “*clock_pad_net*”
  TIMEGRP “*register_group*”;

  where

  - *pad_group* is the user- created group of input pads
  - *time* is the time allowed for the data to propagate from the pad to meet a setup requirement to the clock. This value is in relationship to the clocks initial edge at the pin of the chip. (The PERIOD constraint defines the clock initial edge.)
  - *units* is ms, us, ns (default) or ps
  - *clock_pad_net* is the name of the clock using the net name attached to the pad
  - *register_group* is the user-created group of synchronous elements

- Group OFFSET OUT Example

  TIMEGRP “*pad_group*” **OFFSET = OUT** *time units* **AFTER** “*clock_pad_net*”
  TIMEGRP “*register_group*”;

  where

  - *pad_group* is the user- created group of output pads
  - *time* is the time allowed for the data to propagate from the pad to meet a setup requirement to the clock. This value is in relationship to the clocks initial edge at the pin of the chip. (The PERIOD constraint defines the clock initial edge.)
  - *units* is ms, us, ns (default) or ps
  - *clock_pad_net* is the name of the clock using the net name attached to the pad
  - *register_group* is the user-created group of synchronous elements

FROM TO Syntax

This group includes FROM, TO, and FROM TO. FROM specifies the source group, and TO specifies the destination group. Using just a FROM assumes all destinations are TO points and using just a TO assumes all sources are FROM points. The FROM TO syntax is used in the following path assignments and is defined as follows in the UCF:

TIMESPEC “TS*id*” **= FROM** “*from_grp*” **TO** “*to_grp*” *value units*;

where

- *id* is a user-specified unique identifier for the constraint
- *from_grp* and *to_grp* are TIMEGRPs
- *value* is a specific time, a (*,?) function of another TS*id* (that is, TS_01 *2), or TIG. The allowable operations are: “*” (multiply) and “ / ” (divide).
- *units* is ms, us, ns (default) or ps

Open FROM to TO example:

TIMESPEC “TS*id*” **= FROM** “*from_grp*” *value units*;

where

- *id* is a user specified unique identifier for the constraint
- *from_grp* is TIMEGRP
- *value* is the time requirement
- *units* is ms, us, ns (default) or ps

FROM THRU TO Syntax

You can further narrow down paths by using TPTHRU and FROM THRU TO. You can also specify multiple THRUs. See "TPTHRU". Again, the FROM or TO are optional.

Multi-Cycle Paths Assignments

You can specify multi-cycle path assignments by identifying the start point and end point groups and then applying a FROM TO constraint for that path. For elements controlled by clock enables, use a TNM_NET on the clock enable to identify all of the elements. You can specify timing requirements as a function of the clock. Be aware of your specified units on the originating TSid. If in "MHz", "*" used as multiplication will make the new clock specification faster, if in "ns", "*" will make new clock specification slower.

```
TIMESPEC "TSid" = FROM "from_grp" TO "to_grp" TS_01*2;
```

Slow or Fast Exception Paths

Specify slow or fast path assignments by identifying the start point and end point groups and then applying a FROM TO constraint with a specific value for that path.

```
TIMESPEC "TSid" = FROM "from_grp" TO "to_grp" value units;
```

False Paths by Path

Create groups, specify the FROM TO constraint, and then use TIG as the path value.

```
TIMESPEC "TSid" = FROM "from_grp" TO "to_grp" TIG;
```

Special Case Path Constraining

Special case path constraining allows you to further refine path specifications or define asynchronous points as a path endpoint. TPTHRU allows the further refinement of a FROM TO path. With TPSYNC, you can specify an asynchronous point as a path start or end point.

TPTHRU

TPTHRU narrows the paths constrained by a FROM TO constraint. It specifies nets or instances that the paths must pass through. You can specify multiple TPTHRU points for a set of paths.

TPTHRU Syntax:

There are three forms of the TPTHRU syntax: one identifies THRU points that pass through nets, one identifies THRU points through instances and, finally, one identifies THRU points of specific instance pins. Be careful when placing TPTHRU points as they can get subsumed into components and may not resolve uniquely. The use of the KEEP attribute on the net may be needed to preserve the TPTHRU tag.

- NET Form (UCF)

  ```
  NET "net_name" TPTHRU = "thru_name";
  ```

  where

  - *net_name* is the name of the net the paths pass through
  - *thru_name* is the user name for the THRU point

- INSTANCE Form (UCF)

  INST “*inst_name*” **TPTHRU = “***thru_name*”;

  where

  - *inst_name* is the name of the instance the paths pass through
  - *thru_name* is the user name for the THRU point
- Pin Form (UCF)

  PIN “*instance.pin_name*” **TPTHRU = “***thru_name*”;

  where

  - *instance.pin_name* is the name of the specific instance pin the paths pass through
  - *thru_name* is the user name for the THRU point

FROM THRU TO Syntax (UCF):

TIMESPEC “TS*id*” **= FROM “***from_grp*” **THRU “***thru_point*” **TO “***to_grp*” *value units*;

where

- *id* is a user specified unique identifier for the constraint
- *from_grp* and *to_grp* are TIMEGRPs
- *thru_point* is specified by the TPTHRU tag
- *value* is a number or a (*, /) function of another TSid (i.e. TS_01 *2) or a TIG
- *units* is (ms, us, ns (default) or ps)

You can specify multiple sequential THRU points for any FROM TO specification.

TPSYNC

TPSYNC identifies asynchronous points in the design as endpoints for paths. You may want to use TPSYNC when specifying timing to a non-synchronous point in a path, such as a TBUF or to black box macro pins. You can identify non-synchronous elements or pins as a group, and then use either FROM or TO points.

TPSYNC Syntax:

INST “*inst_name*” **TPSYNC = “***tpsync_name*”;

PIN “*inst_name.pin_name*” **TPSYNC = “***tpsync_name*”;

where

- *tpsync_name* represents the user label for the group that is created by the TPSYNC statement.
- *pin_name* must match the name used in the HDL code or from the library.

Output Slew Rate Constraint

You can use a slew rate of FAST in architectures that support this feature. Outputs are defined as SLOW by default. You can speed up timing by using the FAST property, but this may cause ringing or noise problems.

Following is the slew rate syntax:

INST “*pad_inst_name*” **FAST;**

NET “*pad_net_name*” **FAST;**

where

- *pad_inst_name* is the name of the pad instance
- *pad_net_name* is the name of the pad net. (The port name in HDL code.)

Path Coverage Statistics

A connection is a driver/load pin combination, which is connected by a signal. There are situations where connections are not valid or do not show up in the coverage statistic.

Ignored Paths (TIG)

The most common reason for connection coverage not hitting 100% is that elements in the design have NET TIGs. If the timing tool encounters a TIG'd element when tracing a path, the trace will stop there, possibly leaving connections on the "other side" of the element uncovered. On the other hand, a FROM TO TIG on a path will have all of its connections accounted for in the coverage statistic as those paths are enumerated in the timing report.

STARTUP Paths

There are other reasons for less than 100% coverage. One is that the total number of connections in a design includes some which cannot be covered by constraints. An example is the connections on the STARTUP component.

Static Paths

A static pin can drive a LUT which combines with no other signals and then drives other logic. This can happen at the start of a carry chain where a FORCE mode is used from a logic 1 or 0.

Also if terms for carry logic are connected to a CLB, but are not used within the CLB, these connections will never be traced. These are just obscure cases that are not handled.

Path Tracing Controls

Certain categories of paths are turned off using path tracing controls. Paths that are turned off due to path tracing controls will not be covered. See the ENABLE constraint for more information.

OFFSETs with Derived or Gated Clocks

If the clock that clocks a synchronous element does not come through an input pad -- for example, it is derived from another clock -- then OFFSET will fail to return any paths. Use FROM TOs for these paths, taking into account the clock delay.

Following is an example for pad to setup:

If the global clock delay is 1 ns and the Pad to Setup requirement is 30 ns, then identify the PADs and registers that are clocked by a derived or gated clock and group them accordingly. Then create a similar timing constraint to the following:

```
TIMESPEC “TS_P2S_halfclock” = FROM “halfclock_pads” TO “halfclock_ffs”
31 ns;
```

Static Timing Analysis

You can perform timing analysis at several stages in the implementation flow to show your design delays. You create or generate the following:

- A post-map timing report to evaluate the effects of logic delays on timing constraints.
- A post-place-and-route timing report that incorporates both block and routing delays as a final analysis of the design's timing constraints.

The Interactive Timing Analyzer tool produces detailed timing constraint, clock, and path analysis for post-map or post-place-and-route implementations.

Static Timing Analysis after Map

Post-map timing reports can be very useful in evaluating timing performance. Although route delays are not accounted for, the logic delays can provide valuable information about the design.

If logic delays account for a significant portion (> 50%) of the total allowable delay of a path, the path may not be able to meet your timing requirements when routing delays are added.

Routing delays typically account for 45% to 65% of the total path delays. By identifying problem paths, you can mitigate potential problems before investing time in place and route. You can redesign the logic paths to use fewer levels of logic, tag the paths for specialized routing resources, move to a faster device, or allocate more time for the path.

If logic-only-delays account for much less (<35%) than the total allowable delay for a path or timing constraint, then the place-and-route software can use very low placement effort levels. In these cases, reducing effort levels allow you to decrease runtimes while still meeting performance requirements.

Static Timing Analysis after Place and Route

Post-PAR timing reports incorporate all delays to provide a comprehensive timing summary. If a placed and routed design has met all of your timing constraints, then you can proceed by creating configuration data and downloading a device. On the other hand, if you identify problems in the timing reports, you can try fixing the problems by increasing the placer effort level, using re-entrant routing, or using multi-pass place and route. You can also redesign the logic paths to use fewer levels of logic, tag the paths for specialized routing resources, move to a faster device, or allocate more time for the paths.

Detailed Timing Analysis

To perform detailed timing analysis, select your project in the Sources window, then double click Timing Analyzer under Launch Tools in the Processes window from the Project Navigator. You can specify specific paths for analysis, discover paths not affected by timing constraints, and analyze the timing performance of the implementation based on another speed grade.

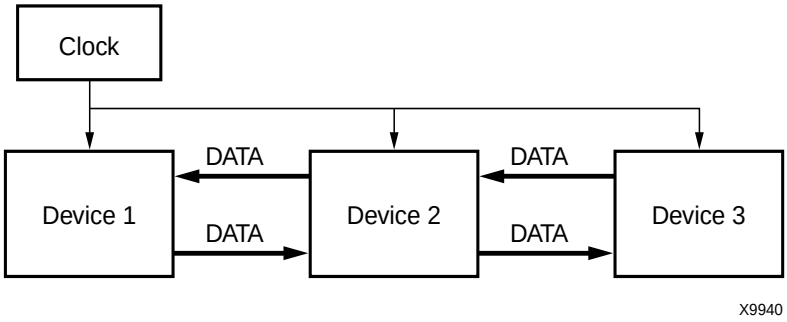
For details, see the Timing Analyzer's online help.

Synchronous Timing

Xilinx supports system synchronous and source synchronous timing. This section describes both types of timing and the keywords INPUT_JITTER, SYSTEM_JITTER, and VALUE. INPUT_JITTER and SYSTEM_JITTER can be used with both system synchronous and source synchronous timing. VALUE can only be used with source synchronous timing

System Synchronous Timing

In system synchronous timing, one clock source controls the data transmission and reception of all devices. See the following diagram.



Source Synchronous Timing

The section describes how to use SYSTEM_JITTER, INPUT_JITTER, and VALUE for source synchronous timing.

In the following example of source synchronous timing, one clock source controls the data transmission of devices. The derived clocks control data reception. See the following diagram.

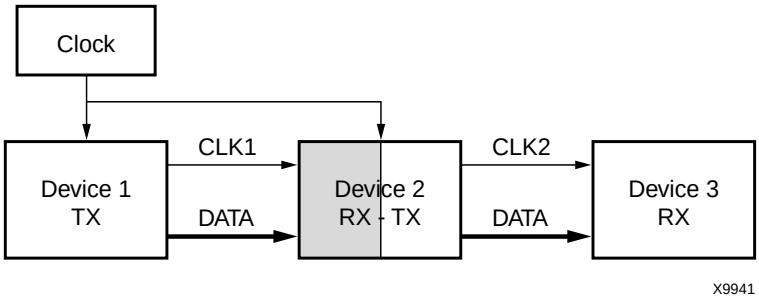
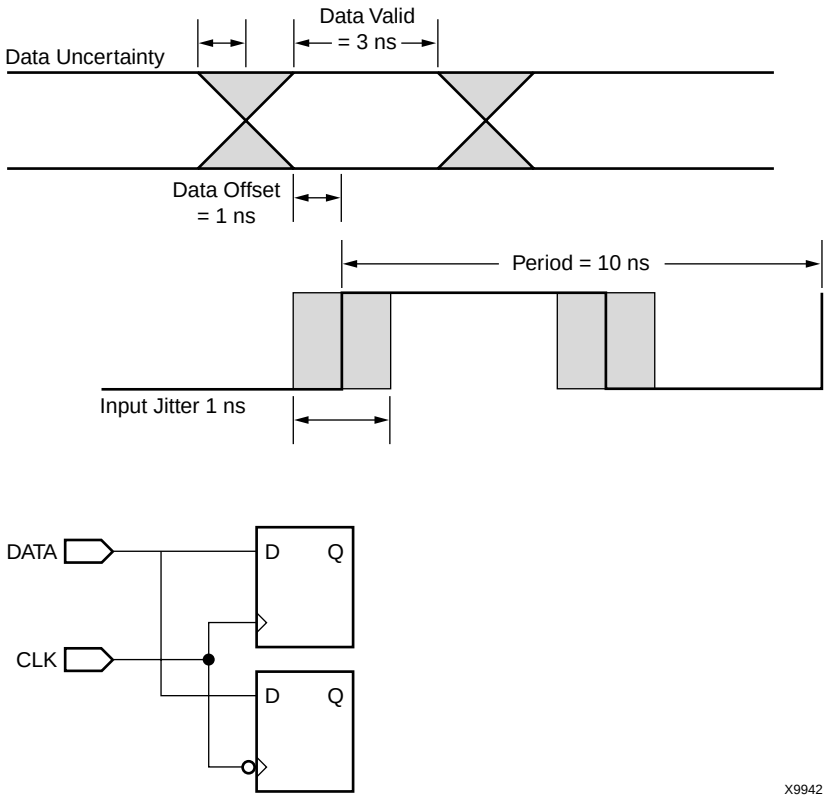


Figure 4-1: **Example of Source Synchronous Timing**

In the preceding example, CLK1 and CLK2 are derived clocks that control data reception of Device 2 and Device 3. The primary clock controls the data transmission for all three devices.

You can use source synchronous timing constraints for Double Data Rate (DDR) or Single Data Rate (SDR) inputs or outputs. The following figure shows an example of a timing diagram for Dual Data Rate inputs for two flip-flops, one with an active High input and one with an active Low input.



The following steps show an example of how to use the PERIOD, OFFSET, and SYSTEM_JITTER constraints for source synchronous timing for the example circuit.

1. Create Period

   ```
   NET CLK TNM_NET = CLK_GRP;
   TIMESPEC "TS_CLK" = PERIOD ”CLK_GRP" 10 ns INPUT_JITTER 1;
   ```

2. Create Groups

   ```
   INST DATA_IN[*] TNM = DATA_IN;
   TIMEGRP FF_RISING = RISING CLK_GRP ;
   TIMEGRP FF_FALLING = FALLING CLK_GRP;
   ```

3. Create OFFSET constraint

   ```
   TIMEGRP DATA_IN OFFSET IN = 1 VALID 3 BEFORE CLK TIMEGRP FF_RISING;
   TIMEGRP DATA_IN OFFSET IN = 4 VALID 3 BEFORE CLK  TIMEGRP FF_FALLING;
   ```

4. Create SYSTEM_JITTER constraint.

   ```
   SYSTEM_JITTER=0.456 ns;
   ```

Directed Routing

Directed Routing is a means of supporting repeatable, locked routing functionality similar to "exact guide" for a limited number of critical signals in a design via UCF constraints. Directed Routing is also used on signals with a limited fanout between comps in close proximity to one another thus avoiding the use of long-line resources. Avoiding long-line resources in Directed Routing constraints is important for two reasons:

- Using such an "expensive" routing resource for a low fanout net is generally a bad practice
- Using long-line resources reduces routing flexibility as the design changes and grows in the design process.

You set the value of the constraint in the FPGA Editor for Directed Routing.

What is Directed Routing?

Directed Routing is:

- A mechanism of locking the routing in order to maintain timing of nets in a design.
- A potential work around for routing limitations.
- A means of controlling route delays to a tighter tolerance than is possible via timing constraints.

How Does Directed Routing Work?

A constraint describing the exact routing resources used to route between source COMP pin(s) and load COMP pin(s) for the selected NET is created.

COMP placement constraints are required to maintain the relative positioning between all COMPs attached to the NET. For SLICE COMPs BEL constraints are also required.

When Should Directed Routing Be Used?

Use Directed Routing in the following circumstances:

- When timing must be maintained (less than 200 ps variation) between implementations on a few nets.
- When both the source and destination comps can be an (R)LOC and BEL constrained to maintain relative placement.
- When skew must be controlled between nets.
- When creating a high-speed macro to limit timing variation between instances of the MACRO.
- When creating a high-speed macro to use in other devices of the same device family.

When Should Directed Routing Not Be Used?

Do not use Directed Routing in the following circumstances:

- When creating a MACRO that uses global resources and will be relocated in the device or other devices in the same device family.
- When routing for hundreds of nets between COMPs must be maintained. Directed Routing is NOT a replacement for Guide.

Related Constraints

- BEL
- LOC
- RLOC
- RLOC_ORIGIN
- U_SET

Chapter 5

Third-Party Constraints

A third party constraint is a constraint from a company other than Xilinx that is supported within the Xilinx technology. This chapter contains the following sections.

Synplicity Constraints

This section describes Synplicity constraints and directives available with Xilinx technology. For more information, see the *Synplicity Synthesis Reference Manual* (http://www.synplicity.com/literature/pdf/syn_ref.pdf), especially Chapter 7, "Synthesis Attributes and Directives," and Appendix H, "Designing with Xilinx."

Table 5-1: **Synplicity Constraints**

Constraint	XST Equivalent	Automatic Recognition	Description
black_box_pad_pin	NA	No	Specifies that a pin on a black box is an I/O pad. It is applied to a component, architecture, or module, with a value that specifies the set of pins on the module or entity.
black_box_tri_pins	NA	No	Specifies that a pin on a black box is a 3-state pin. It is applied to a component, architecture, or module, with a value that specifies the set of pins on the module or entity.
define_clock	period	No	Defines a clock with a specific frequency or clock period goal, and duty cycle.
define_clock_delay	NA	No	Set edge-to-edge clock delay.

Table 5-1: **Synplicity Constraints *(Continued)***

Constraint	XST Equivalent	Automatic Recognition	Description
define_false_path: syn_false_path_start/_end/_through	tig	No	Defines paths to ignore (remove) during timing analysis and assign lower (or no) priority during optimization.
define_input_delay: syn_input_delay, syn_input_delay_improve, syn_input_delay_route	offset_in_before	No	Specifies the input delay, which is the delay consumed outside of the chip before the signal arrives at the input pin.
define_multicycle_path: syn_multicycle_path_start/_end/_through	NA	No	Specifies the paths to use multiple clock cycles.
define_output_delay: syn_output_delay, syn_output_delay_improve, syn_output_delay_route	offset_out_after	No	Specifies the delay of the logic outside the FPGA driven by the outputs.
define_reg_input_delay: syn_reg_input_delay_improve, syn_reg_input_delay_route	NA	No	Speeds up paths feeding a register by a given number of nanoseconds.
define_reg_output_delay: syn_reg_output_delay_improve, syn_reg_output_delay_route	NA	No	Speeds up paths coming from a register by a given number of nanoseconds.
full_case	full_case	No	Specifies that a Verilog case statement has covered all possible cases.
parallel_case	parallel_case	No	Specifies a parallel multiplexed structure in a Verilog case statement, rather than a priority-encoded structure.
syn_black_box	box_type	Yes	Specifies that a module or component is a black box with only its interface defined for synthesis.
syn_direct_enable	NA	No	Controls the assignment of a clock enable net to the dedicated enable pin of a storage element. This is only valid for XC4000 and Virtex architectures.

Table 5-1: **Synplicity Constraints *(Continued)***

Constraint	XST Equivalent	Automatic Recognition	Description
syn_edif_bit_format	NA	No	Controls the character formatting and style of bus signal names, port names, and vector ranges in the EDIF output file.
syn_edif_scalar_format	NA	No	Controls the character formatting of scalar signal and port names in the EDIF output file.
syn_encoding	fsm_encoding	Yes Note: “Safe” value is not supported for automatic recognition. Please use “safe_implementation ” constraint in XST to activate this mode.	Specifies the encoding style for state machines.
syn_enum_encoding	enum_encoding	No	Specifies the encoding style for enumerated types (VHDL only).
syn_hier	keep_hierarchy	Yes Note: Only “hard” and “remove” values are supported for automatic recognition.	Controls the handling of hierarchy boundaries of a module or component during optimization and mapping.
syn_isclock	N/A	No	Specifies that a black box input port is a clock, even if the name does not indicate it is one.
syn_keep	keep	Yes	Prevents the internal signal from being removed during synthesis and optimization.
syn_maxfan	max_fanout	Yes	Sets a fanout limit for an individual input port or register output.
syn_netlist_hierarchy	keep_hierarchy	No	Determines if the EDIF output netlist is flat or hierarchical.
syn_noarrayports	NA	No	Prevents the ports in the EDIF output netlist from being grouped into arrays, and leaves them as individual signals.

Table 5-1: **Synplicity Constraints *(Continued)***

Constraint	XST Equivalent	Automatic Recognition	Description
syn_noclockbuf	buffer_type	Yes	Controls the automatic insertion of global clock buffers.
syn_noprune	optimize_primitives	Yes	Controls the automatic removal of instances that have outputs that are not driven.
syn_pipeline	NA (via register balancing)	No	Specifies that registers be moved into ROMs or multipliers to improve frequency. This only applies to XC4000 and Virtex families.
syn_preserve	equivalent_register_removal	Yes	Prevents sequential optimizations across a flip-flop boundary during optimization, and preserves the signal.
syn_probe	NA	No	Adds probe points for testing and debugging.
syn_ramstyle	ram_extract, ram_style	No	Determines the way in which RAMs are implemented.
syn_reference_clock	NA	No	Specifies a clock frequency other than that implied by the signal on the clock pin of the register. This only applies to the XC4000 and Virtex families.
syn_replicate	register_duplication	Yes	Controls register replication during optimization process.
syn_romstyle	NA	No	Determines how ROM architectures are implemented. This attribute applies to the XC4000 and Virtex families.
syn_sharing	resource_sharing	No	Specifies resource sharing of operators.
syn_state_machine	fsm_extract	No	Determines if the FSM Compiler extracts a structure as a state machine.
syn_tco*n*	NA	No	Defines timing clock to output delay through the black box. The *n* indicates a value between 1 and 10.

Table 5-1: **Synplicity Constraints *(Continued)***

Constraint	XST Equivalent	Automatic Recognition	Description
syn_tpd*n*	NA	No	Specifies timing propagation for combinatorial delay through the black box. The *n* indicates a value between 1 and 10.
syn_tristate	NA	No	Specifies that a black box pin is a 3-state pin.
syn_tristatetomux	NA	No	Converts 3-state drivers that drive nets below a certain limit to muxes. This only applies to the XC4000 and Virtex families.
syn_tsu*n*	NA	No	Specifies the timing setup delay for input pins, relative to the clock. The *n* indicates a value between 1 and 10.
syn_useenables	NA	No	Prevents generation of registers with clock enable pins.
syn_useioff	iob	No	Packs flip-flops in the I/Os to improve input/output path timing. This applies to the XC4000 and Virtex families.
synthesis translate_off/ synthesis translate_on	translate_off/ translate_on	Yes	Specifies sections of code to exclude from synthesis, such as simulation-specific code.
xc_alias	NA	No	Changes the cell name in EDIF for all families except Virtex families.
xc_clockbuftype	buffer_type	No	Specifies that a clock port use the Clock Delay Locked Loop primitive, CLKDLL, in Virtex designs.
xc_fast	NA	No	Speeds up the transition time of the output driver in XC4000 designs.
xc_fast_auto	fast	No	Controls the instantiation of fast output buffers in Virtex designs.
xc_global_buffers	bufg	No	Controls the number of global buffers to use in a design.

Table 5-1: **Synplicity Constraints *(Continued)***

Constraint	XST Equivalent	Automatic Recognition	Description
xc_isgsr	NA	No	Specifies that a black box port is connected to an internal STARTUP block in non-Virtex designs, and prevents Synplify from inferring a STARTUP block.
xc_loc	loc	Yes	Specifies the placement of ports and design units.
xc_map	LUT_MAP	Yes Note: Only “lut” value is supported for automatic recognition.	Specifies the Xilinx the LUT in Virtex designs. See also xc_uset and xc_rloc.
xc_ncf_auto_relax	NA	No	Controls the automatic relaxation of constraints that are forward-annotated to the *.ncf file. This attribute applies to the XC4000 and Virtex families.
xc_nodelay	nodelay	No	Controls the Xilinx insertion of input delay for flip-flops and latches in the XC4000 family.
xc_padtype	iostandard	No	Specifies an I/O buffer standard in Virtex designs.
xc_props	NA	No	Specifies Xilinx attributes to forward to the gate-level netlist.
xc_pullup/xc_pulldown	pullup/ pulldown	No	Specifies that a port is a pull-up or pulldown port.
xc_rloc	rloc	Yes	Specifies the relative locations of all instances with the same xc_uset attribute value. This attribute applies to XC4000 and Virtex families. See also xc_uset and xc_map.
xc_slow	NA	No	Specifies a slow transition time for the driver of an output port (for XC4000).
xc_uset	u_set	Yes	Assigns a group name to component instances. See also xc_rloc and xc_map.

Synopsys Constraints

The following is a list of attributes and directives supported by Synopsys FPGA Express. See the Synopsys documentation for details.

VHDL Directives

- translate_off
- translate_on
- synthesis_off
- synthesis_on
- map_to_entity
- return_port_name
- built_in

VHDL Attributes

- async_set_reset
- sync_set_reset
- async_set_reset_local
- sync_set_reset_local
- async_set_reset_local_all
- sync_set_reset_local_all
- enum_encoding
- one_hot
- one_cold

Verilog Directives

- translate_off
- translate_on
- map_to_module
- return_port_name
- full_case
- parallel_case
- async_set_reset
- sync_set_reset
- async_set_reset_local
- sync_set_reset_local
- async_set_reset_local_all
- sync_set_reset_local_all
- one_hot
- one_cold

Exemplar Constraints

The following is a list of Xilinx-specific attributes supported by Exemplar:

- Assigning the BUFGDLL cell to a clock port

  PAD clk BUFGDLL

  or

  set_attribute clk -name PAD -value BUFGDLL -port
- Assigning a single register to an IOB

  set_attribute reg_state(4) -instance -name IOB -value TRUE
- Setting a Max Fanout on a net

  set_attribute -net sensor2_int -name max_fanout -value 3
- Controlling Block RAM Inference on an instance

  set_attribute -instance .work.u2 -name block_ram -value FALSE
- Forcing a Clock Buffer on an internal net

  set_attribute -net sensor2_int -name PAD -value BUFGP

Some Xilinx-specific optimization variables and their default values are listed below.

To change a variable, use the **set** command (for example, **set lut_max_fanout 6**). These variables affect the entire design during optimization.

- Enables BGSR processing for the Virtex family

  virtex_infer_gsr = FALSE
- Maps to IOB registers for Virtex

  virtex_map_iob_registers = FALSE
- Maps to SRL cells

  virtex_map_srl = TRUE
- Packs SRL cells into a single slice

  virtex_map_srl_pack = TRUE
- Maps to Wide clusters for Virtex

  virtex_map_wide_clusters = TRUE
- Maps to MUXCY for Xilinx Virtex / Virtex-E

  map_muxcy = TRUE
- Specifies the net's fanout for LUT technologies

  lut_max_fanout = 15
- Prints CLB packing [HBLKNM] info in XNF / EDIF, if available

  write_clb_packing = FALSE
- Maps to IOB registers for Virtex

  virtex_map_iob_registers = FALSE
- During optimization, the follow attribute automatically bubbles 3-states to a level of hierarchy wherein all drivers become visible, or to a top-level if the boundary is 3-state.

  bubble_tristates = FALSE

For an example of how to insert Xilinx attributes inside HDL, please refer to Xilinx Solution Record 8074.

Chapter 6

Alphabetized List of Xilinx Constraints

This chapter contains all of the individual constraints. For each constraint, the following information is given.

- Description
- Architecture support
- Applicable elements
- Propagation rules
- Syntax examples for the various constraint entry methods, where applicable

  -- Schematic

  -- VHDL

  -- Verilog

  -- ABEL

  -- NCF

  -- UCF

  -- XCF

  -- Constraints Editor

  -- PCF

  -- Floorplanner

  -- PACE

  -- FPGA Editor

  -- XST command line

  -- Project Navigator

AREA_GROUP

AREA_GROUP Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

AREA_GROUP Applicable Elements

Logic blocks

Timing groups (See “AREA_GROUP -- Defining From Timing Groups”.)

AREA_GROUP Description

AREA_GROUP is a design implementation constraint that enables partitioning of the design into physical regions for mapping, packing, placement, and routing. It can be used in Modular and Incremental Design flows, or can be used during a full compilation of the design to improve design performance.

AREA_GROUP is attached to logical blocks in the design, and the string value of the constraint identifies a named group of logical blocks that are to be packed together by mapper and placed in the ranges if specified by PAR. If AREA_GROUP is attached to a hierarchical block, all sub-blocks in the block are assigned to the group.

Once defined, an AREA GROUP can have a variety of additional constraints associated with it to control its implementation. See the AREA GROUP syntax section for more details.

AREA_GROUP Propagation Rules

The following rules apply to AREA_GROUP.

- When attached to a design element, AREA_GROUP is propagated to all applicable elements in the hierarchy below the component.
- It is illegal to attach AREA_GROUP to a net, signal, or pin.

AREA_GROUP Syntax

The basic UCF syntax for defining an area group is:

```
INST "X" AREA_GROUP=groupname;
```

The syntax to be used in attaching constraints to an area group are:

```
AREA_GROUP "groupname" RANGE=range;
```

or

```
AREA_GROUP "groupname " COMPRESSION=percent;
```

or

```
AREA_GROUP "groupname "IMPLEMENT={FORCE|AUTO};
```

or

```
AREA_GROUP "groupname " GROUP={OPEN|CLOSED};
```

or

```
AREA_GROUP "groupname" PLACE={OPEN|CLOSED};
```

or

```
AREA_GROUP "groupname" MODE={RECONFIG};
```

where

- *groupname* is the name assigned to an implementation partition to uniquely define the group.

Each of these additional area group constraints is described in detail below.

RANGE

RANGE is used to define the range of device resources that are available to place logic contained in the area group, in the same manner ranges are defined for the LOC constraint. (See "AREA_GROUP/RANGE Constraint" for details on how to use RANGE with modular designs.) For Partial Reconfiguration flows, RANGE also restricts the area of routing resources used to implement the area group.

For Spartan-II, Spartan -IIE, Virtex, Virtex-E devices, *range* syntax is as follows:

RANGE=CLB_R*m1*Cn1:CLB_r*m2*C*n2*

RANGE=TBUF_R*m1*Cn1:TBUF_r*m2*C*n2*

RANGE=RAMB4_R*m1*Cn1:RAMB4_r*m2*C*n2*

For Spartan-3, Spartan-3E, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4 devices, range syntax is as follows:

RANGE=SLICE_X*m1*Yn1:SLICE_x*m2*Y*n2*

RANGE=TBUF_X*m1*Yn1:TBUF_X*m2*Y*n2*

RANGE=MULT18X18_X*m1*Yn1:MULT18X18_X*m2*Y*n2*

RANGE=RAMB16_X*m1*Yn1:RAMB16_X*m2*Y*n2*

Note: TBUF is not supported by Spartan-3, Spartan-3E, and Virtex-4.

Virtex, Virtex-E, Virtex-II, Virtex-II Pro, Virtex-II Pro X, Virtex-4, Spartan-II, Spartan-IIE, Spartan-3, Spartan-3E devices and CLBS / SLICEs are supported. If an area group contains both TBUFs (not applicable for Spartan -3) and one for CLBs / SLICEs, two separate AREA_GROUP RANGEs can be specified: one for TBUFs and one for CLBs / SLICEs.

You can use the wildcard character for either the row number or column number. For Spartan-3, Spartan-3E, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4 you can use the wildcard character for either the X coordinate or the Y coordinate.

COMPRESSION

COMPRESSION defines the compression factor for the area groups. The percent values can be from 0 to 100. If the AREA_GROUP does not have a RANGE, only 0 (no compression) and 1 (maximum compression) are meaningful. The mapper computes the number of CLBs in the AREA_GROUP from the *range* and attempts to compress the logic into the percentage specified. Compression does not apply to TBUFs, BRAMs, nor multipliers.

The compression factor is similar to the -c option in MAP, except that it operates on the area group instead of the whole design. Area group compression interacts with the -c map option as follows:

- Area groups with a compression factor are not affected by the -c option. (Logic that is not part of an AREA_GROUP is not merged with grouped logic if the AREA_GROUP has its own compression factor.)
- AREA_GROUPs without a compression factor are affected by the -c option. The mapper may attempt to combine ungrouped logic with logic that is part of an area group without a compression factor.
- At no time is the logic from two separate AREA_GROUPs combined.
- The -c map option does not force compression among slices in the same area group.

The Map Report (MRP) includes a section that summarizes area group processing.

If a symbol that is part of an AREA_GROUP contains a LOC constraint, the mapper removes the symbol from the area group and processes the LOC constraint.

Note: Logic that does not belong to any AREA_GROUP can be pulled into the region of logic belonging to an area group, as well as being packed or merged with such logic to form SLICES.

IMPLEMENT

For IMPLEMENT, the string value must be one of the following:

- FORCE -- Forces the AREA_GROUP logic to be re-implemented.
- AUTO -- Determines if the AREA_GROUP logic has changed and, if so, the logic is reimplemented.

  The default is AUTO.

GROUP

GROUP controls the packing of logic into physical components (i.e., slices) as follows:

- CLOSED -- Do not allow logic *outside* the AREA_GROUP to be combined with logic *inside* the AREA_GROUP
- OPEN -- Allow logic outside the AREA_GROUP to be combined with logic inside the AREA_GROUP
- Default values for various flows:
  - Default flow: GROUP=OPEN
  - Modular flow: GROUP=CLOSED
  - Partial Reconfiguration flow: GROUP=CLOSED
  - Incremental flow: GROUP=CLOSED

Note: That GROUP=OPEN is illegal in all modular and Partial Reconfiguration flows and will result in an error. GROUP defaults to CLOSED for incremental design flows in the 6.1i release.

PLACE

PLACE controls the allocation of resources in the area group's RANGE, as follows:

- CLOSED -- Do not allow comps that are not members of the AREA_GROUP to be placed within the RANGE defined for the AREA_GROUP.
- OPEN -- Allow comps that are not members of the AREA_GROUP to be placed within the RANGE defined for the AREA_GROUP.
- Default values for various flows:
  - Default flow: PLACE=OPEN
  - Modular flow: PLACE=OPEN
  - Partial Reconfiguration flow: PLACE=CLOSED
  - Incremental flow: PLACE=OPEN

See "AREA_GROUP / PLACE Constraint" for details on how to use PLACE with modular designs.

MODE

MODE is used to define a reconfigurable area group, as in the following example:

- MODE=RECONFIG

See "AREA_GROUP / MODE Constraint" for details on how to use MODE with partially reconfigurable designs.

AREA_GROUP Examples

Schematic

Attach AREA_GROUP=*groupname* to a valid instance.

Attach RANGE =*range* to a CONFIG symbol.

Attach COMPRESSION=*percent* to a CONFIG symbol.

Attach IMPLEMENT={**FORCE** | **AUTO**} to a CONFIG symbol.

Attach GROUP={**OPEN** | **CLOSED**} to a CONFIG symbol.

Attach PLACE={**OPEN** | **CLOSED**} to a CONFIG symbol.

Attach to a CONFIG symbol. For a value of TRUE, PLACE, and GROUP must both be CLOSED.

Attribute Names—AREA_GROUP, RANGE *range*, COMPRESSION *percent*, IMPLEMENT={**FORCE** | **AUTO**}, GROUP={**OPEN** | **CLOSED**}, PLACE={**OPEN** | **CLOSED**}, and MODE={**RECONFIG**}.

Attribute Values—*groupname*, *range*, *percent*, IMPLEMENT={**FORCE** | **AUTO**}, GROUP={**OPEN** | **CLOSED**}, PLACE={**OPEN** | **CLOSED**}, MODE={**RECONFIG**}

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

For architectures with slice-based XY designations (Spartan-3, Spartan-3E, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4 only)

The following example assigns all the logical blocks in state_machine_X to the area group "group1" and places CLB logic in the physical area between CLB 1,1 and CLB 10,10. It places TBUFs in the physical area between TBUF 1,0 and TBUF 10,10. Unrelated logic within "group1" will not be compressed. Because compression is defined, ungrouped logic will not be combined with logic in "group1."

```
INST “state_machine_X” AREA_GROUP=group1;
AREA_GROUP “group1” COMPRESSION=0;
AREA_GROUP “group1” RANGE=CLB_R1C1:CLB_R10C10;
AREA_GROUP “group1” RANGE=TBUF_X6Y0:TBUF_X10Y22; (Not applicable for Spartan-3)
```

Note: Spartan-3 does not have any TBUF resources.

The following example assigns all the logical blocks in state_machine_X to the area group, "group1," and places logic in the physical area bounded by SLICE_X3Y1 in the lower left corner and SLICE_X33Y33 in the upper left corner. It places TBUFs in the physical area

bounded by TBUF_X6Y0 and TBUF_X10Y22. Unrelated logic within "group1" will *not* be compressed. Because compression is defined, ungrouped logic will *not* be combined with logic in "group1."

```
INST “state_machine_X” AREA_GROUP=group1;
AREA_GROUP “group1” COMPRESSION=0;
AREA_GROUP “group1” RANGE=SLICE_X3Y1:SLICE_X33Y33;
AREA_GROUP “group1” RANGE=TBUF_X6Y0:TBUF_X10Y22;
```

The following example assigns I$1, I$2, I$3, and I$4 to the area group "group2." Because there is no compression, ungrouped logic may be combined within this area group.

```
INST “I$1” AREA_GROUP=group2;
INST “I$2” AREA_GROUP=group2;
INST “I$3” AREA_GROUP=group2;
INST “I$4” AREA_GROUP=group2;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

See the “Using a Floorplanner UCF File in Project Navigator,” “Assigning Area Constraints for Modular Design," and “Creating and Editing Area Constraints” topics in the Advanced Procedures section of the Floorplanner online help.

PACE

The Pin AREA Constraints Editor is mainly used to identify and assign areas to hierarchical blocks of logic. You can access PACE from the Processes window in the Project Navigator. Double-click Create Area Constraints.

For details on how to use PACE, see the PACE online help, especially the topic “Editing Area Constraints.”

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

AREA_GROUP -- Modular Design Use

The following sections explain how to use AREA_GROUP in modular designs.

INST/AREA_GROUP constraint

The following sections explain how to use AREA_GROUP in modular designs.

The INST / AREA_GROUP UCF constraint has the following syntax:

```
INST "X" AREA_GROUP="name";
```

A unique AREA_GROUP value must be attached to each module in the design. This group will be translated into some number of COMPGRP constraints in the PCF file. A unique COMPGRP constraint will be defined with SLICEs, TBUFs and BRAMs depending upon whether or not any INSTs of these types are found underneath the logical node X. Each COMPGRP will contain all of the components containing the referenced logic. The format of these constraints is:

```
COMPGRP "name.slice" COMP "c1" COMP "c2" ... ;
```

Where components c1, c2 ... are all components of type SLICE that contains logic underneath the logical node X.

Certain operations can then be performed on this group of logic. Within the modular design flow, the INST / AREA_GROUP constraint is used to define a module.

AREA_GROUP/RANGE Constraint

The AREA_GROUP / RANGE UCF constraint can have 2 syntaxes:

Syntax 1:

```
AREA_GROUP "name" RANGE="start:end";
```

The preceding syntax specifies that all logic of the AREA_GROUP name should be located in the region of the target chip with a lower left corner of start and an upper right corner of end. The start and end parameters are specified relative to the target architecture type (Spartan-3, Virtex-II Virtex-II Pro, Virtex-II Pro X, and Virtex-4 use X*Y* while Virtex uses R*C* syntax) and the component type (SLICE, TBUF or RAM16). This AREA_GROUP / RANGE constraint will be translated into a COMPGRP / LOCATE constraint in the PCF file. This PCF file has the following syntax:

```
COMPGRP "name" LOCATE = SITE "start:end";
```

Within the modular design flow the AREA_GROUP / RANGE constraint is used to place all logic of a module into the given area. No logic from the top-level design context or any other module will be permitted to be placed within the defined area.

The following site type names are legal with the associated value:

- *CLB logic_range*:

  Specifies a range of sites in the target chip for logic. The format is CLB_R*C*:CLB_R*C* for Virtex, Virtex-E, Spartan-II, Spartan-IIE, and SLICE_X*Y*:SLICE_X*Y* for Spartan-3, Spartan-3E, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4.

  The asterisk (*) indicates any valid index number.

- BRAM *bram_range*:

  Specifies a range of sites in target chip for block rams. The format is RAMB4_R*C*:RAMB4_R*C* for Virtex, Virtex-E, Spartan-II, Spartan-IIE, and

RAMB16_X*Y*:RAMB16_X*Y* for Spartan-3, Spartan-3E, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4. The index numbers supplied do not directly correlate to the those indices used for logic or TBUFs.

- TBUF *tbuf_range*:

  Specifies a range of sites in the target chip for TBUFs. Format is TBUF_R*C*:TBUF_R*C* for Virtex, Virtex-E, Spartan-II, Spartan-IIE, and TBUF_X*Y*:TBUF_X*Y* for Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4. The index numbers supplied do not directly correlate to the those indices used for logic or brams.

- IOB *iob_range*:

  This will be a colon-separated list of IOB sites that are legal for use by this module.

When used in modular designs, all routing that connects only members of an area group will be constrained to lie within the range.

Syntax 2:

This syntax is supported for all INST types that can be used in AREA_GROUP constraints.

For Spartan-3, Spartan-3E, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4, AREA_GROUP is supported for various clock regions:

For a single region:

```
AREA_GROUP "group_name" RANGE = CLOCKREGION_X#Y#;
```

For a range of clock regions that form a rectangle:

```
AREA_GROUP "group_name" RANGE = CLOCKREGION_X#Y#:CLOCKREGION_X#Y#;
```

For a list of clock regions:

```
AREA_GROUP "group_name" RANGE = CLOCKREGION_X#Y#,CLOCKREGION_X#Y#,...;
```

The valid X# and Y# values vary by device. For Spartan-3, Spartan-3E, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4, the X value is 0 or 1 for all devices, while the Y value is 0 through 7, depending on the device.

AREA_GROUP/PLACE Constraint

The syntax for this constraint for modular designs is:

```
AREA_GROUP "group_name" PLACE=CLOSED;
```

PAR reads the value CLOSED and does not allow comps outside the AREA_GROUP to be within the RANGE specified for the AREA_GROUP.

AREA_GROUP/MODE Constraint

PAR reads the value RECONFIG and uses only those routing resources that can be driven within the reconfigurable region.

The syntax for this constraint for modular designs is:

```
AREA_GROUP “"group_name" MODE={RECONFIG};
```

MODE=RECONFIG identifies the AREA_GROUP as a partially reconfigurable region. When implementing a design for Partial Reconfiguration, all AREA GROUPs should have the MODE=RECONFIG constraint to ensure that the reconfiguration process does not affect the behavior of the static (non-reconfigurable) portions of the design.

AREA_GROUP -- Incremental Design Use

The following sections explain how to use AREA_GROUP in Incremental Designs.

For best results in an Incremental Design flow, a unique AREA_GROUP value should be associated with hierarchical instances of the design that are to be used. TIMEGRP-based AREA_GROUPs and AREA_GROUPs defined by tagging more than one instance in the design with the same value may not yield consistent insulation between implementation regions, and thus may not result in the best runtime or preservation of implementation for unchanged portions of the design. To minimize the impact on overall design performance, each hierarchical instance marked as an AREA GROUP should have its output signals registered. AREA_GROUPs should be top-level instantiations.

AREA_GROUP/GROUP Constraint

The syntax for this constraint for Incremental Designs is:

AREA_GROUP "*group_name***" GROUP=CLOSED|OPEN;**

By default, AREA_GROUPs are CLOSED in incremental design, ensuring the best possible insulation of implementation. Setting GROUP=OPEN may improve overall design performance, but may also result in more of the design being reimplemented when a small change is made to the design.

AREA_GROUP/PLACE Constraint

The syntax for this constraint for Incremental Designs is:

AREA_GROUP "*group_name***" PLACE=CLOSED|OPEN;**

AREA GROUPs are open to placement by default in incremental flows. Setting PLACE=CLOSED may improve the consistency with which design performance is met for that group, but may also increase the overall device utilization requirements for the design.

AREA_GROUP/IMPLEMENT Constraint

The syntax for this constraint in incremental design is:

AREA_GROUP "*group_name***" IMPLEMENT=FORCE|AUTO;**

The default value is AUTO, which will cause the implementation tools to determine when an AREA_GROUP needs to be reimplemented, based on detection of a design change or a change to AREA_GROUP constraint values, such as RANGE, COMPRESSION, etc. Use IMPLEMENT=FORCE to force the tools to reimplement an AREA_GROUP when they would otherwise have retained the previous implementation, i.e., some other constraint, such as a timing specification, has changed.

AREA_GROUP -- Partial Reconfiguration

The following sections explain how to use AREA_GROUP with Partial Reconfiguration.

Partial reconfiguration may be achieved on some Xilinx devices by using the modular design flows and constraints described above, and invoking the MODE=RECONFIG constraint. This constraint should be specified on all AREA_GROUPs in a design employing Partial Reconfiguration. All other aspects of modular design apply to Partial Reconfiguration flows can be set in PACE.

AREA_GROUP -- Defining From Timing Groups

You can create an area group based on a timing group by using the following UCF or NCF syntax:

```
TIMEGRP timing_group_name AREA_GROUP = area_group_name;
```

where *timing_group_name* is the name of a previously defined timing group, and *area_group_name* is the name of a new area group to be defined from the TIMEGRP contents. This is equivalent to manually assigning each member of the timing group to area_group_name. The area group name defined by this statement can be used in RANGE constraints, just like any other area group name.

In the AREA_GROUP definition, the timing_group_name will generally be that of a TNM_NET group, which allows area groups to be formed based on the loads of clock or other control nets. (AREA_GROUPs defined in this way are not suitable for either Modular nor Incremental design. Defining AREA_GROUPs from TIMEGRPs is useful for improving placement of designs with many different clock domains in devices that have more clocks than clock regions.)

You can also specify a TNM group name, or the name of a user group defined by a TIMEGRP statement (but note that edge qualifiers used in the TIMEGRP definition are ignored when determining area group membership). In all cases, the AREA_GROUP members are determined after the TIMEGRP has been propagated to its target elements.

Since TIMEGRPs can contain only synchronous elements and pads, area groups defined from timing groups will also contain only these element types. If an AREA_GROUP is defined by a TIMEGRP that contains only flip-flops or latches, assigning a RANGE to that group makes sense only if ungrouped logic is also allowed within the area. Therefore, COMPRESSION should not be defined for such groups.

If a TNM_NET is used by a PERIOD specification, and is traced into a Virtex, Virtex-E, Spartan-II, Spartan-IIE, CLKDLL or Spartan-3, Spartan-3E, Virtex-II, Virtex-II Pro, Virtex-II Pro X, Virtex, or Vitex-4, DCM, new TNM_NET groups and PERIOD specifications are created at the CLKDLL or DCM outputs. If the original TNM_NET is used to define an area group, and if more than one clock tap is used on the CLKDLL or DCM, the area group will be split into separate groups at each clock tap.

For example, assume you have the following UCF constraints:

```
NET "clk" TNM_NET="clock";
TIMESPEC "TS_clk" = PERIOD "clock" 10 MHz;
TIMEGRP "clock" AREA_GROUP="clock_area";
```

If the net clk is traced into a CLKDLL or DCM, a new group and PERIOD specification will be created at each clock tap. Likewise, a new area group will also be created at each clock tap, with a suffix indicating the clock tap name. If the CLK0 and CLK2X taps were used, the AREA_GROUPS clock_area_CLK0 and clock_area_CLK2X would be defined automatically.

When AREA_GROUP definitions are split in this manner, NGDBuild will issue an informational message, showing the names of the new groups. These new group names, rather than the originally specified one, should be used in RANGE constraints.

ASYNC_REG

ASYNC_REG Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

ASYNC_REG Applicable Elements

This constraint can only be attached to registers and latches and should only be used on registers or latches with asynchronous inputs (D input or the CE input).

ASYNC_REG Description

This timing constraint improves the behavior of asynchronously clocked data for simulation. Specifically, it disables 'X' propagation during timing simulation. In the event of a timing violation, the previous value is retained on the output instead of going unknown.

ASYNC_REG Propagation Rules

Applies to the register or latch to which it is attached.

ASYNC_REG Syntax Examples

Schematic

Not applicable.

VHDL

Before using ASYNC_REG, declare it with the following syntax:

```
attribute ASYNC_REG : string;
```

After ASYNC_REG has been declared, specify the VHDL constraint as follows:

```
attribute ASYNC_REG of signal_name|instance_name: label is
"{TRUE|FALSE}";
```

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
// synthesis attribute ASYNC_REG [of] signal_name|instance_name: is
"{TRUE|FALSE}";
```

For a more detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

```
INST "instance_name" ASYNC_REG = {TRUE|FALSE};
```

The default (if constraint is not applied) is FALSE. If no boolean value is supplied it is considered TRUE.

XCF

Not applicable.

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints. You can set using the Misc tab.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

BEL

BEL Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

BEL Applicable Elements

- Registers
- FMAP
- LUTs
- SRL16s
- XORCY
- RAM16XLS
- IFF1
- IFF2
- OFF1
- OFF2
- TFF1
- TFF2

BEL Description

BEL is an advanced placement constraint. It locks a logical symbol to a particular BEL site in a slice, or an IOB. BEL differs from LOC in that LOC allows specification to the comp level. BEL allows specification as to which particular BEL site of the or IOB slice is to be used.

An IOB BEL constraint does not direct the mapper to pack the register into an IOB component. Some other feature (the -pr switch, for example) must cause the packing. Once the register is directed to an IOB, the BEL constraint will cause the proper placement within the IOB.

BEL Propagation Rules

It is illegal to attach BEL to a net or signal.

BEL Syntax Examples

Schematic

Attached to a valid instance.

Attribute Name—BEL

Attribute Values—F, G, FFX, FFY, XORF, XORG

VHDL

Before using BEL, declare it with the following syntax:

```
attribute bel : string;
```

After BEL has been declared, specify the VHDL constraint as follows:

```
attribute bel of {component_name|label_name}: {component|label} is
"{F|G|FFX|FFY|XORF|XORG}";
```

See UCF / NCF for a description of the BEL values.

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute bel [of] {module_name|instance_name} [is]
{F|G|FFX|FFY|XORF|XORG};
```

See the UCF / NCF section for a description of the BEL values.

For a more detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

The syntax is:

```
INST "instance_name" BEL={F | G |FFX | FFY | XORF | XORG};
```

where

- F and G identify specific LUTs, SRL16s, distributed RAM components in the slice
- FFX and FFY identify specific flip-flops, latches, etc. in a slice
- XORF and XORG identify XORCY elements in a slice

The following statement locks **xyzzy** to the FFX site on the slice.

```
INST "xyzzy" BEL=FFX;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

BLKNM

BLKNM Architecture Support

The numbers indicate the applicable elements (see the next section).

Architecture	Supported/Unsupported
Virtex	1, 2, 3, 4, 5, 6, 7
Virtex-E	1, 2, 3, 4, 5, 6, 7
Spartan-II	1, 2, 3, 4, 5, 6, 7
Spartan-IIE	1, 2, 3, 4, 5, 6, 7
Spartan-3	1, 2, 3, 5, 6, 7
Spartan-3E	1, 2, 3, 5, 6, 7
Virtex-II	1, 2, 3, 4, 5, 6, 7
Virtex-II Pro	1, 2, 3, 4, 5, 6, 7
Virtex-II Pro X	1, 2, 3, 4, 5, 6, 7
Virtex-4	1, 2, 3, 5, 6, 7
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

BLKNM Applicable Elements

1. Flip-flop and latch primitives
2. Any I/O element or pad
3. FMAP
4. BUFT
5. ROM primitives
6. RAMS and RAMD primitives
7. Carry logic primitives

Note: You can also attach BLKNM to the net connected to the pad component in a UCF file. NGDBuild transfers the constraint from the net to the pad instance in the NGD file so that it can be processed by the mapper. Use the following syntax:

```
NET "net_name" BLKNM=property_value;
```

BLKNM Description

BLKNM is an advanced mapping constraint. BLKNM assigns block names to qualifying primitives and logic elements. If the same BLKNM constraint is assigned to more than one instance, the software attempts to map them into the same block. Conversely, two symbols with different BLKNM names are not mapped into the same block. Placing similar BLKNMs on instances that do not fit within one block creates an error.

Specifying identical BLKNM constraints on FMAP tells the software to group the associated function generators into a single CLB. Using BLKNM, you can partition a complete CLB without constraining the CLB to a physical location on the device.

BLKNM constraints, like LOC constraints, are specified from the design. Hierarchical paths are not prefixed to BLKNM constraints, so BLKNM constraints for different CLBs must be unique throughout the entire design. See the section on the HBLKNM constraint for information on attaching hierarchy to block names.

BLKNM allows any elements except those with a different BLKNM to be mapped into the same physical component. Elements without a BLKNM can be packed with those that have a BLKNM. See XBLKNM for information on allowing only elements with the same XBLKNM to be mapped into the same physical component.

BLKNM Propagation Rules

When attached to a design element, it is propagated to all applicable elements in the hierarchy within the design element.

BLKNM Syntax Examples

Schematic

Attach to a valid instance.

Attribute Name—BLKNM

Attribute Value—*block_name*

VHDL

Before using BLKNM, declare it with the following syntax:

```
attribute blknm: string;
```

After BLKNM has been declared, specify the VHDL constraint as follows:

```
attribute blknm of
{component_name|signal_name|entity_name|label_name}:
{component|signal|entity|label} is "block_name";
```

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute blknm [of]
{module_name|instance_name|signal_name} [is] blk_name;
```

For a more detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST “instance_name” BLKNM=block_name;
```

where *block_name* is a valid block name for that type of symbol.

For information on assigning hierarchical block names, see “HBLKNM”.

The following statement assigns an instantiation of an element named block1 to a block named U1358.

```
INST “$1I87/block1” BLKNM=U1358;
```

XCF

```
MODEL “entity_name” blknm = block_name;

BEGIN MODEL “entity_name”
 INST "instance_name" blknm = block_name;
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

BOX_TYPE

BOX_TYPE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

BOX_TYPE Applicable Elements

The constraint applies to the following design elements:

VHDL: component, entity

Verilog: module, instance

XCF: model, instance

BOX_TYPE Description

BOX_TYPE is a synthesis constraint. It currently takes three possible values: *primitive*, *black_box*, and *user_black_box*, which instruct XST not to synthesize the behavior of a module. Please note that the *black_box* value is equivalent to *primitive* and will eventually become obsolete.

The main difference between the *primitive* (*black_box*) and *user_black_box* is that if the *user_black_box* value is specified, XST reports inference of a black box in the LOG file, but XST doesn't do this if the *primitive* value is specified.

Please not that if the *box_type* is applied to at least a single instance of a block at a particular hierarchical level, then *box_type* is propagated to all other instances of this block at this hierarchical level. This feature was implemented for Verilog and XCF only in order to have a VHDL-like support, where *box_type* can be applied on a component.

BOX_TYPE Propagation Rules

Applies to the design element to which it is attached.

BOX_TYPE Syntax Examples

Schematic

Not applicable.

VHDL

Before using BOX_TYPE, declare it with the following syntax:

```
attribute box_type: string;
```

After BOX_TYPE has been declared, specify the VHDL constraint as follows:

```
attribute box_type of {component_name|entity_name}: {component|entity}
is "{primitive|black_box|user_black_box}";
```

For a more detailed discussion of the basic VHDL syntax, see "VHDL"

Verilog

Specify as follows:

```
 // synthesis attribute box_type [of] {module_name|instance_name} [is]
"{primitive|black_box|user_black_box}";
```

For a more detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

NCF/UCF

Not applicable.

XCF

```
MODEL "entity_name" box_type="{primitive|black_box|user_black_box}";
BEGIN MODEL "entity_name"
 INST "instance_name" box_type="{primitive|black_box|user_black_box}";
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

BRAM_MAP

BRAM_MAP Architecture Support

The following table lists supported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

BRAM_MAP Applicable Elements

BRAMs

BRAM_MAP Description

BRAM_MAP is an XST mapping constraint that will map user logic to block RAM. It is similar to the FSM_Style constraint, but applies to all user logic, not just state machines. The values are Yes and No, with No being the default. This is both a global and a local constraint.

BRAM_MAP Propagation Rules

The user must isolate the logic (including output register) to be mapped on ram in a separate hierarchical level. The logic must fit on a single block ram, otherwise it will not be mapped on block ram. Pay attention that the whole entity must fit, not just part of it.

The attribute BRAM_MAP is set on the instance or entity. If no block ram can be inferred, the logic is passed to the global optimization that will optimize it. The macros *will not* be inferred. Pay close attention as to whether or not XST has mapped the logic.

BRAM_MAP Syntax Examples

Schematic

Not applicable.

VHDL

Before using BRAM_MAP, declare it with the following syntax:

```
attribute BRAM_MAP: string;
```

After BRAM_MAP has been declared, specify the VHDL constraint as follows:

```
attribute BRAM_MAP of component_name: component is
“{yes|no|true|false}”;
```

For a more detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
 // synthesis attribute BRAM_MAP [of] module_name [is]
{yes|no|true|false};
```

For a more detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

Not applicable.

UCF

Not applicable.

NCF

Not applicable.

XCF

```
MODEL “entity_name” BRAM_MAP = {yes|no|true|false};

BEGIN MODEL “entity_name”
 INST "instance_name" BRAM_MAP = {yes|no|true|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

BUFFER_TYPE

BUFFER_TYPE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

BUFFER_TYPE Applicable Elements

Signals

BUFFER_TYPE Description

BUFFER_TYPE is a synthesis constraint that will eventually replace CLOCK_BUFFER. It selects the type of buffer to be inserted on the input port or internal net

Please note that “bufr” value is supported for Virtex-4 device family only.

BUFFER_TYPE Propagation Rules

Applies to the signal to which it is attached.

BUFFER_TYPE Syntax Examples

Schematic

Not applicable.

VHDL

Before using BUFFER_TYPE, declare it with the following syntax:

```
attribute buffer_type: string;
```

After BUFFER_TYPE has been declared, specify the VHDL constraint as follows:

```
attribute buffer_type of signal_name: signal is
"{bufgdll|ibufg|bufgp|ibuf|bufr|none}";
```

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify BUFFER_TYPE as follows:

```
 // synthesis attribute buffer_type [of] signal_name [is]
{bufgdll|ibufg|bufgp|ibuf|bufr|none};
```

For a detailed discussion of Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF

Not applicable.

NCF

Not applicable.

XCF

```
BEGIN MODEL "entity_name"
 NET "signal_name"  buffer_type={bufgdll|ibufg|bufgp|ibuf|bufr|none};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

BUFG (CPLD)

BUFG (CPLD) Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	No
Spartan-3E	No
Virtex-II	No
Virtex-II Pro	No
Virtex-II Pro X	No
Virtex-4	No
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes*
CoolRunner-II	Yes
* OE, SR not supported.	

BUFG (CPLD) Applicable Elements

Any input buffer (IBUF), input pad net, or internal net that drives a CLK, OE, SR, DATA_GATE pin.

BUFG (CPLD) Description

BUFG is an advanced fitter constraint and a synthesis constraint. When applied to an input buffer or input pad net, the BUFG attribute maps the tagged signal to a global net. When applied to an internal net, the tagged signal is either routed directly to a global net or brought out to a global control pin to drive the global net, as supported by the target device family architecture.

BUFG (CPLD) Propagation Rules

When attached to a net, BUFG has a net or signal form and so no special propagation is required. When attached to a design element, BUFG is propagated to all applicable elements in the hierarchy within the design element.

BUFG (CPLD) Syntax Examples

Schematic

Attach to an IBUF instance of the input pad connected to an IBUF input.

Attribute Name—BUFG

Attribute Values—CLK, OE, SR, DATA_GATE

BUFG=CLK: maps to a global clock (GCK) line.

BUFG=OE: maps to a global 3-state control (GTS) line.

BUFG=SR: maps to a global set/reset control (GSR) line.

BUFG=DATA_GATE: maps to the DataGate latch enable control line.

VHDL

Before using BUFG, declare it with the following syntax:

```
attribute BUFG: string;
```

After BUFG has been declared, specify the VHDL constraint as follows:

```
attribute BUFG of signal_name: signal is "{CLK|OE|SR|DATA_GATE}";
```

BUFG=CLK: maps to a global clock (GCK) line.

BUFG=OE: maps to a global 3-state control (GTS) line.

BUFG=SR: maps to a global set/reset control (GSR) line.

BUFG=DATA_GATE: maps to the DataGate latch enable control line.

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify BUFG as follows:

```
 // synthesis attribute BUFG [of] signal_name [is]
{CLK|OE|SR|DATA_GATE}
```

BUFG=CLK: maps to a global clock (GCK) line.

BUFG=OE: maps to a global 3-state control (GTS) line.

BUFG=SR: maps to a global set/reset control (GSR) line.

BUFG=DATA_GATE: maps to the DataGate latch enable control line.

For a detailed discussion of Verilog syntax, see "Verilog".

ABEL

```
XILINX PROPERTY 'bufg={clk|oe|sr|DATA_GATE} signal_name';
```

UCF/NCF

The basic UCF syntax is

```
NET “net_name” BUFG={CLK | OE | SR | DATA_GATE};
INST “instance_name” BUFG={CLK | OE | SR | DATA_GATE};
```

where

- CLK designates a global clock pin (all CPLD families).
- OE designates a global 3-state control pin (all CPLDs except CoolRunner) or internal global 3-state control line (CoolRunner-II only).
- SR designates a global set/reset pin (all CPLDs except CoolRunner).
- DATA_GATE: maps to the DataGate latch enable control line.

The following statement maps the signal named **fastclk** to a global clock net.

```
NET “fastclk” BUFG=CLK;
```

XCF

```
BEGIN MODEL “entity_name”
 NET "signal_name" BUFG = {CLK|OE|SR|DATA_GATE};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

BUFGCE

BUFGCE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

BUFGCE Applicable Elements

Clock signals

BUFGCE Description

BUFGCE is a synthesis constraint that implements BUFGMUX functionality by inferring a BUFGMUX primitive.

This operation reduces the wiring: clock and clock enable signals are driven to N sequential components by a single wire.

This constraint must be attached to the primary clock signal and may have two values: **yes**, **no**. This constraint is accessible through HDL code. If **bufgce=yes**, then XST will implement BUFGMUX functionality if possible (all flip-flops must have the same clock enable signal).

BUFGCE Propagation Rules

Applies to the signal to which it is attached.

BUFGCE Syntax Examples

Schematic

Not applicable.

VHDL

Before using BUFGCE, declare it with the following syntax:

```
attribute bufgce : string;
```

After BUFGCE has been declared, specify the VHDL constraint as follows:

```
attribute bufgce of signal_name: signal is "{yes(no)}";
```

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify BUFGCE as follows:

```
// synthesis attribute bufgce [of] signal_name [is] yes
```

For a detailed discussion of Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
BEGIN MODEL "entity_name"
 NET "primary_clock_signal"
 bufgce={yes|no|true|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

CLK_FEEDBACK

CLK_FEEDBACK Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes*
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No
* See the latest published errata sheets for current information regarding this use.	

CLK_FEEDBACK Applicable Elements

DCM (Digital Clock Manager)

CLK_FEEDBACK Description

CLK_FEEDBACK is a basic DLL / DCM constraint. It specifies the feedback clock source as either the CLK0, CLK2X output, or none.

CLK_FEEDBACK Propagation Rules

It is illegal to attach CLK_FEEDBACK to a net or signal. When attached to a DCM, CLK_FEEDBACK is propagated to all applicable elements of the DCM.

CLK_FEEDBACK Syntax Examples

Schematic

Attach to a DCM instance.

Attribute Name—CLK_FEEDBACK

Attribute Values—1X, 2X, NONE

VHDL

Before using CLK_FEEDBACK, declare it with the following syntax:

```
attribute clk_feedback: string;
```

After CLK_FEEDBACK has been declared, specify the VHDL constraint as follows:

```
attribute clk_feedback of {component_name|label_name}:
{component|label} is "{1X|2X|NONE}";
```

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute clk_feedback [of] {module_name|instance_name}
[is] "{1X|2X|NONE}";
```

For a more detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name" CLK_FEEDBACK={1X|2X|NONE};
```

where

- 1X, the default, indicates that the CLK0 output is the source for feedback.
- 2X indicates that the CLK2X output is the source for feedback.
- NONE indicates the CLKFB is unconnected. The valid outputs are CLKFX and CLKFX180. These outputs are generated without phase correction with respect to CLKIN.

CLK_FEEDBACK is always 1X when DLL_FREQUENCY_MODE=HIGH. NONE must be specified when only DFS outputs are used (and, hence, there is no CLKFB connection) in order for the simulation models to function correctly.

When DLL_FREQUENCY_MODE=LOW, the following statement specifies the use of the CLK2X output as the feedback source.

```
INST "foo/bar" CLK_FEEDBACK=2X;
```

For Virtex-4, CLKFEEDBACK=NONE can be used with DCM output (not just CLKFX/FX180). The output is not de-skewed to CLKIN. For Virtex II and Virtex II Pro, you can do it only for CLKFX/FX180.

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

CLOCK_BUFFER

CLOCK_BUFFER Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

CLOCK_BUFFER Applicable Elements

Signals

CLOCK_BUFFER Description

CLOCK_BUFFER is a synthesis constraint that will eventually be replaced by "BUFFER_TYPE.". It selects the type of buffer to be inserted on the input port or internal net.

CLOCK_BUFFER Propagation Rules

Applies to the signal to which it is attached.

CLOCK_BUFFER Syntax Examples

Schematic

Not applicable.

VHDL

Before using CLOCK_BUFFER, declare it with the following syntax:

```
attribute clock_buffer: string;
```

After CLOCK_BUFFER has been declared, specify the VHDL constraint as follows:

```
attribute clock_buffer of signal_name: signal is
"{bufgdll|ibufg|bufgp|ibuf|none}";
```

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify CLOCK_BUFFER as follows:

```
 // synthesis attribute clock_buffer [of] signal_name [is]
{bufgdll|ibufg|bufgp|ibuf|none};
```

For a detailed discussion of Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
BEGIN MODEL "entity_name"
 NET "signal_name"  clock_buffer={bufgdll|ibufg|bufgp|ibuf|none};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

CLOCK_SIGNAL

CLOCK_SIGNAL Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

CLOCK_SIGNAL Applicable Elements

Signals

CLOCK_SIGNAL Description

CLOCK_SIGNAL is a synthesis constraint. In the case where a clock signal goes through combinatorial logic before being connected to the clock input of a flip-flop, XST cannot identify what input pin or internal net is the real clock signal. This constraint allows you to define the clock net.

CLOCK_SIGNAL Propagation Rules

Applies to a clock signal.

CLOCK_SIGNAL Syntax Examples

Schematic

Not applicable

VHDL

Before using CLOCK_SIGNAL, declare it with the following syntax:

```
attribute clock_signal : string;
```

After CLOCK_SIGNAL has been declared, specify the VHDL constraint as follows:

```
attribute clock_signal of signal_name : signal is “yes”;
```

For a more detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute clock_signal [of] signal_name [is] “yes”;
```

For a more detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
BEGIN MODEL “entity_name”
 NET “primary_clock_signal” {clock_signal={yes|no|true|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

CLKDV_DIVIDE

CLKDV_DIVIDE Architecture Support

The numbers in the second column indicate applicable elements. See the section, "CLKDV_DIVIDE Applicable Elements", for a description of "1" and "2".

Architecture	Supported/Unsupported
Virtex	1
Virtex-E	1, 2
Spartan-II	1
Spartan-IIE	1, 2
Spartan-3	2
Spartan-3E	2
Virtex-II	2
Virtex-II Pro	2
Virtex-II Pro X	2
Virtex-4	2
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

CLKDV_DIVIDE Applicable Elements

1. CLKDLL, CLKDLLE (Virtex-E only), CLKDLLHF
2. DCM

CLKDV_DIVIDE Description

CLKDV_DIVIDE is a basic DLL / DCM constraint. It specifies the extent to which the CLKDLL, CLKDLLE, CLKDLLHF, or DCM clock divider (CLKDV output) is to be frequency divided. .

CLKDV_DIVIDE Propagation Rules

It is illegal to attach CLKDV_DIVIDE to a net or signal. When attached to a DCM / DLL, CLK_FEEDBACK is propagated to all applicable elements of the DCM or DLL.

CLKDV_DIVIDE Syntax Examples

Schematic

Attach to a CLKDLL, CLKDLLE, CLKDLLHF, or DCM instance.

Attribute Name—CLKDV_DIVIDE

Attribute Values—1.5, 2.0, 2.5, 3.0, 3.5, 4.0, 4.5, 5.0, 5.5, 6.0, 6.5, 7.0, 7.5, 8.0, 9.0, 10.0, 11.0, 12.0, 13.0, 14.0, 15.0, 16.0

VHDL

Before using CLKDV_DIVIDE, declare it with the following syntax:

```
attribute clkdv_divide: string;
```

After CLKDV_DIVIDE has been declared, specify the VHDL constraint as follows:

```
attribute clkdv_divide of {component_name|label_name}:
{component|label} is
"{1.5|2.0|2.5|3.0|3.5|4.0|4.5|5.0|5.5|6.0|6.5|7.0|7.5
|8.0|9.0|10.0|11.0|12.0|13.0|14.0|15.0|16.0}";
```

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute clkdv_divide [of] {module_name|instance_name}
[is] "{1.5|2.0|2.5|3.0|3.5
|4.0|4.5|5.0|5.5|6.0|6.5|7.0|7.5|8.0|9.0|10.0|11.0|
12.0|13.0|14.0|15.0|16.0}";
```

For a more detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name"
CLKDV_DIVIDE={1.5|2.0|2.5|3.0|3.5|4.0|4.5|5.0|5.5|6.0|6.5|7.0|7.5|
8.0|9.0|10.0|11.0|12.0| 13.0|14.0|15.0| 16.0};
```

The default is 2.0 if no CLKDV_DIVIDE constraint is specified.

For the Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4, DCM, if the CLKDV_DIVIDE value is a non-integer and if the DLL_FREQUENCY_MODE is HIGH, the duty cycle is adjusted as follows:

- 33% HIGH for CLKDV_DIVIDE=1.5
- 40% HIGH for CLKDV_DIVIDE=2.5
- 43% HIGH for CLKDV_DIVIDE=3.5
- 44% HIGH for CLKDV_DIVIDE=4.5
- 45% HIGH for CLKDV_DIVIDE=5.5

- 46% HIGH for CLKDV_DIVIDE=6.5
- 47% HIGH for CLKDV_DIVIDE=7.5

The following statement specifies a frequency division factor of 8 for the clock divider foo/bar.

```
INST “foo/bar” CLKDV_DIVIDE=8;
```

XCF

```
MODEL “entity_name” clkdv_divide=integer;


BEGIN MODEL “entity_name”
 INST "instance_name" clkdv_divide=integer;
END;
```

For valid *integer* values, see the UCF syntax discussion.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not Applicable.

Project Navigator

Not applicable.

CLKFX_DIVIDE

CLKFX_DIVIDE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

CLKFX_DIVIDE Applicable Elements

DCM (Digital Clock Manager)

CLKFX_DIVIDE Description

CLKFX_DIVIDE is a basic DLL / DCM constraint. It specifies the frequency divider value for the CLKFX output. After LOCKED is High, the following equation specifies the CLKFX frequency:

$$\mathbf{Frequency}_{CLKFX} = \mathbf{(CLKFX\_MULTIPLY\_value/CLKFX\_DIVIDE\_value) * Frequency}_{CLKFIN}$$

CLKFX_DIVIDE Propagation Rules

It is illegal to attach CLKDV_DIVIDE to a net. When attached to a DCM, CLKDV_DIVIDE is propagated to all applicable elements of the DCM.

CLKFX_DIVIDE Syntax Examples

Schematic

Attach to a DCM instance.

Attribute Name—CLKFX_DIVIDE

Attribute Value—*n*

where *n* is an integer that falls within the specified range of the data sheet. The default is 1.

VHDL

Before using CLKFX_DIVIDE, declare it with the following syntax:

```
attribute clkfx_divide: integer;
```

After CLKFX_DIVIDE has been declared, specify the VHDL constraint as follows:

```
attribute clkfx_divide of {component_name|label_name}:
{component|label} is "n";
```

where *n* is an integer from 1 through 4096. The default is 1.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute clkfx_divide [of] {module_name|instance_name}
[is] "n";
```

where *n* is an integer from 1 through 4096. The default is 1.

For a detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name" CLKFX_DIVIDE=n;
```

where *n* is an integer between 1 and 4096. The default is 1. Floating-point values (for example, 1.0) are not acceptable.

Assuming that CLKFX_MULTIPLY is defaulted to 4, the following statement specifies that the frequency at CLKFX is one-half of the CLKIN frequency.

```
INST "foo/bar" CLKFX_DIVIDE=8;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Select a DCM component from the List window. Click editblock from the User toolbar that is located to the right of the List window. Click the F= button to display CLKFX_DIVIDE in the lower portion of the Block window.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

CLKFX_MULTIPLY

CLKFX_MULTIPLY Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

CLKFX_MULTIPLY Applicable Elements

DCM (Digital Clock Manager)

CLKFX_MULTIPLY Description

CLKFX_MULTIPLY is a basic DLL / DCM constraint. It specifies the frequency multiplier value for the CLKFX output. After LOCKED is High, the following equation specifies the CLKFX frequency.

$$\mathbf{Frequency_{CLKFX} = (CLKFX\_MULTIPLY\_value/CLKFX\_DIVIDE\_value)*Frequency_{CLKFIN}}$$

CLKFX_MULTIPLY Propagation Rules

It is illegal to attach CLKFX_MULTIPLY to a net or signal. When attached to a DCM, CLKFX_MULTIPLY is propagated to all applicable elements of the DCM.

CLKFX_MULTIPLY Syntax Examples

Schematic

Attach to a DCM instance.

Attribute Name—CLKFX_MULTIPLY

Attribute Value—*n*

where *n* is an integer falls within the specified range of the data sheet. The default is 4.

VHDL

Before using CLKFX_MULTIPLY, declare it with the following syntax:

```
attribute clkfx_multiply: integer;
```

After CLKFX_MULTIPLY has been declared, specify the VHDL constraint as follows:

```
attribute clkfx_multiply of {component_name|label_name}:
{component|label} is "n";
```

where *n* is an integer from 1 through 4096. The default is 4.

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
// synthesis attribute clkfx_multiply [of] {module_name|instance_name}
[is] "n";
```

where *n* is an integer from 1 through 4096. The default is 4.

For a more detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name" CLKFX_MULTIPLY=n;
```

where *n* is an integer falling within the specified range of the data sheet. The default is 4.

Assuming that CLKFX_DIVIDE is defaulted to 1, this statement specifies that the frequency at CLKFX is 8 times the CLKIN frequency.

```
INST "foo/bar" CLKFX_MULTIPLY=8;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Select a DCM component from the List window. Click editblock from the User toolbar that is located to the right of the List window. Click the F= button to display CLKFX_MULTIPLY in the lower portion of the Block window.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

CLKIN_DIVIDE_BY_2

CLKIN_DIVIDE_BY_2 Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

CLKIN_DIVIDE_BY_2 Applicable Elements

DCM

CLKIN_DIVIDE_BY_2 Description

This DCM constraint allows the input clock frequency to be divided in half when such a reduction is necessary to meet the DCM input clock frequency requirements.

CLKIN_DIVIDE_BY_2 Propagation Rules

Applies to the DCM to which it is attached.

CLKIN_DIVIDE_BY_2 Syntax Examples

Schematic

Attach to a DCM instance.

Attribute Name—CLKIN_DIVIDE_BY_2

Attribute Value— {TRUE|FALSE}

The default is FALSE.

VHDL

Before using CLKIN_DIVIDE_BY_2, declare it with the following syntax:

```
attribute clkin_divide_by_2: string;
```

After CLKIN_DIVIDE_BY_2 has been declared, specify the VHDL constraint as follows:

```
attribute clkin_divide_by_2 of {component_name|label_name}:
{component|label} is “true”;
```

For a more detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
 // synthesis attribute clkin_divide_by_2 [of]
{module_name|instance_name} [is] “true”;
```

For a more detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

Not applicable.

UCF

The basic syntax is:

```
INST “instance_name” CLKIN_DIVIDE_BY_2={TRUE|FALSE};
```

The default is FALSE.

NCF

Not applicable.

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

CLKIN_PERIOD

CLKIN_PERIOD Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

CLKIN_PERIOD Applicable Elements

DCM (Digital Clock Manager)

CLKIN_PERIOD Description

CLKIN_PERIOD specifies the period of the clock used to drive the CLKIN pin of the DCM. It must be specified to provide software with enough information for optimal frequency synthesis operation given an M and D value when using the CLKFX or CLKFX180 outputs. It is not needed for other DCM clock outputs.

CLKIN_PERIOD Propagation Rules

It is illegal to attach CLKIN_PERIOD to a net or signal. When attached to a DCM, CLKIN_PERIOD is propagated to all applicable elements of the DCM.

CLKIN_PERIOD Syntax Examples

Schematic

Attach to a DCM instance.

Attribute Name—CLKIN_PERIOD

Attribute Value—*n*

where *n* is a floating point number representing nanoseconds.

VHDL

Before using CLKIN_PERIOD, declare it with the following syntax:

```
attribute clkin_period: real;
```

After CLKIN_PERIOD has been declared, specify the VHDL constraint as follows:

```
attribute clkin_period of {component_name|label_name}:
{component|label} is "n";
```

where *n* is a floating point number representing nanoseconds.

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute clkin_period [of] {module_name|instance_name}
[is] "n";
```

where *n* is a floating point number representing nanoseconds.

For a more detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF

The basic UCF syntax is:

```
INST "instance_name" CLKIN_PERIOD=n;
```

where *n* is a floating point number representing nanoseconds.

The following statement specifies a 35 nanosecond period of the clock used to drive the CLKIN pin of the DCM.

INST "foo/bar" CLKIN_PERIOD=35;

NCF

Not applicable.

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Select a DCM component from the List window. Click editblock from the User toolbar that is located to the right of the List window. Click the F= button to display CLKIN_PERIOD in the lower portion of the Block window..

XST Command Line

Not applicable.

Project Navigator

Not applicable.

CLKOUT_PHASE_SHIFT

CLKOUT_PHASE_SHIFT Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

CLKOUT_PHASE_SHIFT Applicable Elements

DCM (Digital Clock Manager)

CLKOUT_PHASE_SHIFT Description

CLKOUT_PHASE_SHIFT is an advanced DCM constraint. It sets the skew control mode. Together with the PHASE_SHIFT constraint, it implements the Digital Phase Shifter (DPS) feature of the DCM.

CLKOUT_PHASE_SHIFT Propagation Rules

It is illegal to attach CLKOUT_PHASE_SHIFT to a net or signal. When attached to a DCM, CLKOUT_PHASE_SHIFT is propagated to all applicable elements of the DCM.

CLKOUT_PHASE_SHIFT Syntax Examples

Schematic

Attach to a DCM instance.

Attribute Name—CLKOUT_PHASE_SHIFT

Attribute Values—NONE, FIXED, VARIABLE

VHDL

Before using CLKOUT_PHASE_SHIFT, declare it with the following syntax:

```
attribute clkout_phase_shift: string;
```

After CLKOUT_PHASE_SHIFT has been declared, specify the VHDL constraint as follows:

```
attribute clkout_phase_shift of {component_name|label_name}:
{component|label} is "{NONE|FIXED|VARIABLE}";
```

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute clkout_phase_shift [of]
{module_name|instance_name} [is] {NONE|FIXED|VARIABLE};
```

For a more detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name" CLKOUT_PHASE_SHIFT={NONE|FIXED| VARIABLE};
```

where

- NONE, the default, specifies that CLKIN and CLKFB are in phase (no skew) and may not be changed. (This is equivalent to FIXED with a PHASE_SHIFT value of 0.)
- FIXED indicates that the skew is set at configuration and may not be changed later. It instructs the DCM to lock with the CLKIN leading CLKFB by the positive PHASE_SHIFT skew and the CLKIN lagging CLKFB by the negative PHASE_SHIFT skew.
- VARIABLE indicates that the skew is set at configuration but that it may be changed later. It instructs the DCM to lock with the CLKIN leading CLKFB by the positive PHASE_SHIFT skew and the lagging CLKFB by the negative PHASE_SHIFT skew. In addition, you can adjust the PHASE_SHIFT value in increments of +/- 1 using the DCM's PSEN, PSCLK, and PSINCDEC inputs.

For the FIXED and VARIABLE modes, skew is represented by the following equation:

$$CLKIN\_CLKFB\_skew = (PHASE\_SHIFT / 256) * Period_{CLKIN}$$

where PHASE_SHIFT is the value set by the PHASE_SHIFT constraint.

The following statement indicates that the CLKIN / CLKFB skew is set by the PHASE_SHIFT constraint value at configuration and cannot be changed later.

```
INST “foo/bar” CLKOUT_PHASE_SHIFT=FIXED;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

COLLAPSE

COLLAPSE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	No
Spartan-3E	No
Virtex-II	No
Virtex-II Pro	No
Virtex-II Pro X	No
Virtex-4	No
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

COLLAPSE Applicable Elements

Any internal net

COLLAPSE Description

COLLAPSE is an advanced fitter constraint. It forces a combinatorial node to be collapsed into all of its fanouts.

COLLAPSE Propagation Rules

COLLAPSE is a net constraint. Any attachment to a design element is illegal.

COLLAPSE Syntax Examples

Schematic

Attach to a logic symbol or its output net.

Attribute Name—COLLAPSE

Attribute Values—TRUE, FALSE

VHDL

Before using COLLAPSE, declare it with the following syntax:

```
attribute collapse: string;
```

After COLLAPSE has been declared, specify the VHDL constraint as follows:

```
attribute collapse of signal_name: signal is “yes”;
```

For a more detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute collapse [of] signal_name [is] “yes”;
```

For a more detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
NET “net_name” COLLAPSE;
```

The following statement forces net $1N6745 to collapse into all its fanouts.

```
NET “$1I87/$1N6745” COLLAPSE;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

COMPGRP

COMPGRP Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

COMPGRP Applicable Elements

Groups of components

COMPGRP Description

COMPGRP is an advanced grouping constraint and an advanced modular design constraint. It identifies a group of components.

COMPGRP Propagation Rules

Not applicable.

COMPGRP Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

```
COMPGRP "group_name"=comp_item1... comp_itemn [EXCEPT comp_group];
```

where *comp_item* is one of the following,

- **COMP "***comp_name***"**
- **COMPGRP "***group_name***"**

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

COMPGRP for Modular Designs

The AREA_GROUP / RANGE constraint is translated into a COMPGRP / LOCATE constraint in the PCF file. This constraint has the following syntax:

```
COMPGRP "name" LOCATE = SITE "start:end";
```

The INST / AREA_GROUP is translated into some number of COMPGRP constraints in the PCF file. A unique COMPGRP constraint will be defined as SLICEs, TBUFs and BRAMs depending upon whether or not any INSTs of these types are found underneath the logical node X. Each COMPGRP will contain all of the components containing the referenced logic. The format of these constraints is:

```
COMPGRP "name.slice" COMP "c1" COMP "c2" ...;
```

Where components *c1*, *c2* ... are all components of type *slice* that contain logic underneath the logical node X.

See "AREA_GROUP -- Modular Design Use".

CONFIG

CONFIG Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

CONFIG Applicable Elements

Used with PROHIBIT, STEPPING, and VREF.

CONFIG Description

CONFIG can be defined with the following:

- PROHIBIT. See “PROHIBIT”.
- STEPPING

  When the CONFIG STEPPING constraint is specified for an enhanced multiplier, Timing Analyzer and TRCE perform timing analysis based on the enhanced multiplier performance. For a complete description of STEPPING, see the Solution Record 14339.
- VREF. See “VREF”.

CONFIG Propagation Rules

It is illegal to attach CONFIG to a net, signal, entity, module, or macro.

CONFIG Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

The following rules apply:

- The package string must always begin with an alphabetic character — *never* with a number.
- The speed string must always begin with a numeric character —*never* with an alphabetic character.
- The text XC is an optional prefix to the whole *part_type* string.
- In a constraints file, the PART specification must be preceded by the keyword CONFIG.

The following statement prohibits use of the site P45.

```
CONFIG PROHIBIT=P45;
```

For CLB-based Row/Column/Slice Designations

The following statement prohibits use of the CLB located in Row 6, Column 8.

```
CONFIG PROHIBIT=CLB_R6C8;
```

The following statement prohibits use of the site TBUF_R5C2.2.

```
CONFIG PROHIBIT=TBUF_R5C2.2;
```

For Slice-based XY Coordinate Designations

The following statement prohibits use of the slice at the SLICE_X6Y8 site.

```
CONFIG PROHIBIT=SLICE_X6Y8;
```

The following statement prohibits use of the TBUF at the TBUF_X6Y2 site.

```
CONFIG PROHIBIT=TBUF_X6Y2;
```

For support with STEPPING, see Solution Record 14339. Following is a UCF syntax example.

```
CONFIG STEPPING="1";
```

For support with VREF, see “VREF”.

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

For the Part keyword, double-click the part in the Sources window. Select the Device Family and Device in the Project Properties dialog box.

CONFIG_MODE

CONFIG_MODE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

CONFIG_MODE Applicable Elements

Attaches to the CONFIG symbol.

CONFIG_MODE Description

This constraint communicates to PAR which of the dual purpose configuration pins can be used as general purpose IOs.

This constraint is used by PAR to prohibit the use of Dual Purpose IOs if they are required for CONFIG_MODE: S_SELECTMAP+READBACK OR M_SELECTMAP+READBACK.

In the case of CONFIG_MODE: S_SELECTMAP OR M_SELECTMAP, PAR uses the Dual Purpose IOs as General Purpose IOs only if necessary.

CONFIG_MODE Propagation Rules

Applies to dual-purpose I/Os.

CONFIG_MODE Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF

The basic UCF syntax is:

```
CONFIG CONFIG_MODE=string;
```

where *string* can be one of the following:

S_SERIAL = Slave Serial Mode

M_SERIAL = Master Serial Mode (The default value)

S_SELECTMAP = Slave SelectMAP Mode

M_SELECTMAP = Master SelectMAP Mode.

B_SCAN = Boundary Scan Mode

S_SELECTMAP+READBACK = Slave SelectMAP Mode with Persist set to support Readback and Reconfiguration.

M_SELECTMAP+READBACK = Mater SelectMAP Mode with Persist set to support Readback and Reconfiguration.

B_SCAN+READBACK = Boundary Scan Mode with Persist set to support Readback and Reconfiguration.

NCF

Not applicable.

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

COOL_CLK

COOL_CLK Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	No
Spartan-3E	No
Virtex-II	No
Virtex-II Pro	No
Virtex-II Pro X	No
Virtex-4	No
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	Yes

COOL_CLK Applicable Elements

Applies to any input pad or internal signal driving a register clock.

COOL_CLK Description

You can save power by combining clock division circuitry with the DualEDGE circuitry. This capability is called CoolCLOCK and is designed to reduce clocking power within a CPLD. Because the clock net can be an appreciable power drain, the clock power can be reduced by driving the net at half frequency, then doubling the clock rate using DualEDGE triggered macrocells.

COOL_CLK Propagation Rules

Applying COOL_CLK to a clock net is equivalent to passing the clock through a divide-by-two clock divider (CLK_DIV2) and replacing all flip-flops controlled by that clock with

DualEDGE flip-flops. Using the COOL_CLK attribute does not alter your overall design functionality.

Some restrictions are as follows:

- You cannot use COOL_CLK on a clock that triggers any flip-flop on the low-going edge. (The CoolRunner-II clock divider can only be triggered on the high-rising edge of the clock signal.)
- If there are any DualEDGE flip-flops in your design source, the clock that controls any of them cannot be specified as a COOL_CLK.
- If there is already a clock divider in your design source, you cannot also use COOL_CLK. (CoolRunner-II devices contain only one clock divider.)

COOL_CLK Syntax Examples

Schematic

Attach to a input pad or internal signal driving a register clock.

Attribute Name—COOL_CLK

Attribute Values—TRUE, FALSE

VHDL

Before using COOL_CLK, declare it with the following syntax:

```
attribute cool_clk: string;
```

After COOL_CLK has been declared, specify the VHDL constraint as follows:

```
attribute cool_clk of signal_name: signal is “true”;
```

For a more detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute cool_clk [of] signal_name [is] “true”;
```

For a more detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

```
XILINX PROPERTY 'COOL_CLK signal_name';
```

UCF/NCF

```
NET “signal_name” COOL_CLK;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

DATA_GATE

DATA_GATE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	No
Spartan-3E	No
Virtex-II	No
Virtex-II Pro	No
Virtex-II Pro X	No
Virtex-4	No
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	Yes*
* Applies only to devices of 128 macrocells and above.	

DATA_GATE Applicable Elements

I/O pads and pins

DATA_GATE Description

The CoolRunner-II DataGate feature provides direct means of reducing power consumption in your design. Each I/O pin input signal passes through a latch that can block the propagation of incident transitions during periods when such transitions are not of interest to your CPLD design. Input transitions that do not affect the CPLD design function will still consume power, if not latched, as they are routed among the CPLD's Function Blocks. By asserting the DataGate control I/O pin on the device, selected I/O pin

inputs become latched, thereby eliminating the power dissipation associated with external transitions on those pins.

Applying the DATA_GATE attribute to any I/O pad indicates that the pass-through latch on that device pin is to respond to the DataGate control line. Any I/O pad (except the DataGate control I/O pin itself), including clock input pads, can be configured to get latched by applying the DATA_GATE attribute. All other I/O pads that do not have a DATA_GATE attribute remain unlatched at all times. The DataGate control signal itself can be received from off-chip via the DataGate I/O pin, or you can generate it in your design based on inputs that remain unlatched (pads without DATA_GATE attributes).

See "BUFG (CPLD)" for more details on using DATA_GATE with Verilog and VHDL designs.

DATA_GATE Propagation Rules

See "DATA_GATE Description".

DATA_GATE Syntax Examples

Schematic

Attach to I/O pads and pins.

Attribute Name—DATA_GATE

Attribute Values—TRUE, FALSE

VHDL

Before using DATA_GATE, declare it with the following syntax:

```
attribute DATA_GATE : string;
```

After DATA_GATE has been declared, specify the VHDL constraint as follows:

```
attribute DATA_GATE of signal_name: signal is "true";
```

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
// synthesis attribute DATA_GATE [of] signal_name [is] "true";
```

For a more detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

```
XILINX PROPERTY 'DATA_GATE signal_name';
```

NCF

Same as UCF.

UCF

```
NET "signal_name" DATA_GATE;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

XCF

```
BEGIN MODEL "entity_name"
NET "signal_name" data_gate={true|false}";
END;
```

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

DCI_VALUE

DCI_VALUE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

DCI_VALUE Applicable Elements

IOBs

DCI_VALUE Description

DCI_VALUE determines which buffer behavioral models are associated with the IOBs of a design in the generation of an IBS file using IBISWriter.

DCI_VALUE Propagation Rules

Applies to the IOB to which it is attached.

DCI_VALUE Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

```
PIN pin_name DCI_VALUE = integer;
```

Legal values are integers 25 through 100 with an implied units of ohms. The default value is 50 ohms.

Constraints Editor

Not applicable.

PCF

Not applicable.

XCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

DECODER_EXTRACT

DECODER_EXTRACT Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

DECODER_EXTRACT Applicable Elements

Can be applied globally or to an entity, module or signal.

DECODER_EXTRACT Description

DECODER_EXTRACT is a synthesis constraint. It enables or disables decoder macro inference.

DECODER_EXTRACT Propagation Rules

Following is a list of propagation rules.

- When attached to a net or signal, DECODER_EXTRACT applies to the attached signal.
- When attached to an entity or module, DECODER_EXTRACT is propagated to all applicable elements in the hierarchy within the entity or module.

DECODER_EXTRACT Syntax Examples

Schematic

Not applicable.

VHDL

Before using DECODER_EXTRACT, declare it with the following syntax:

```
attribute decoder_extract: string;
```

After DECODER_EXTRACT has been declared, specify the VHDL constraint as follows:

```
attribute decoder_extract of {entity_name|signal_name}:
{entity|signal} is “yes”;
```

For a more detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
 // synthesis attribute decoder_extract [of] {module_name|signal_name}
[is] “yes”;
```

For a more detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL “entity_name” decoder_extract={yes|no|true|false};


BEGIN MODEL “entity_name”
 NET “signal_name” decoder_extract={yes|no|true|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define DECODER_EXTRACT globally with the **-decoder_extract** command line option of the **run** command. Following is the basic syntax:

```
-decoder_extract {YES|NO}
```

The default is **YES**.

Project Navigator

DECODER_EXTRACT can be globally set with the Decoder Extraction option in the HDL Options tab of the Process Properties dialog box within the Project Navigator. Allowed values are **yes** (check box is checked) and **no** (check box in not checked). By default, decoder inference is enabled (check box is checked).

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

DESKEW_ADJUST

DESKEW_ADJUST Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

DESKEW_ADJUST Applicable Elements

DCM

DESKEW_ADJUST Description

This constraint sets configuration bits affecting the clock delay alignment between the DCM output clocks and an FPGA clock input pin. The attribute value should be selected solely based on the type of clocking arrangement used in the customer design, most commonly either SOURCE_SYNCHRONOUS or SYSTEM_SYNCHRONOUS (default).

The clock delay alignment is taken into account in the Tdcmino delay value in the timing report. Tdcmino will be a larger number (i.e., less negative, since Tdcmino is typically negative) when using the SOURCE_SYNCHRONOUS value with the end result of a longer clock delay to the IOB clock input. This will affect the setup and hold times by reducing the input setup time and increasing the input hold time. The overall data sample window

is smaller with SOURCE_SYNCHRONOUS due to the smaller variance in the clock delay through the DCM.

This constraint should not be used to achieve phase shift on DCM clock outputs. Instead, use the CLKOUT_PHASE_SHIFT and PHASE_SHIFT constraints to achieve accurate phase shifting.

DESKEW_ADJUST Propagation Rules

It is illegal to attach DESKEW_ADJUST to a net or signal. When attached to a DCM, the DESKEW_ADJUST constraint is propagated to all applicable elements of the DCM.

DESKEW_ADJUST Syntax Examples

Schematic

Not applicable.

VHDL

Before using DESKEW_ADJUST, declare it with the following syntax:

```
attribute deskew_adjust: string;
```

After DESKEW_ADJUST has been declared, specify the VHDL constraint as follows:

```
attribute deskew_adjust of dcm_instance_name : label is
“{SYSTEM_SYNCHRONOUS|SOURCE_SYNCHRONOUS}”;
```

SYSTEM_SYNCHRONOUS is the default.

For a more detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute deskew_adjust [of] dcm_instance_name [is]
{SYSTEM_SYNCHRONOUS|SOURCE_SYNCHRONOUS};
```

SYSTEM_SYNCHRONOUS is the default.

For a more detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

Not applicable.

UCF

```
INST “foo/bar” DESKEW_ADJUST=SYSTEM_SYNCHRONOUS;
```

NCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

XCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

DFS_FREQUENCY_MODE

DFS_FREQUENCY_MODE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

DFS_FREQUENCY_MODE Applicable Elements

DCM (Digital Clock Manager)

DFS_FREQUENCY_MODE Description

DFS_FREQUENCY_MODE is an advanced DCM constraint. It specifies the frequency range allowed at the CLKIN input and at the output clocks for the DCM's digital frequency synthesizer (DFS).

DFS_FREQUENCY_MODE Propagation Rules

It is illegal to attach DFS_FREQUENCY_MODE to a net or signal. When attached to a DCM, DFS_FREQUENCY_MODE is propagated to all applicable elements of the DCM.

DFS_FREQUENCY_MODE Syntax Examples

Schematic

Attach to a DCM instance.

Attribute Name—DFS_FREQUENCY_MODE

Attribute Values—LOW, HIGH

VHDL

Before using DFS_FREQUENCY_MODE, declare it with the following syntax:

```
attribute dfs_frequency_mode: string;
```

After DFS_FREQUENCY_MODE has been declared, specify the VHDL constraint as follows:

```
attribute dfs_frequency_mode of {component_name|label_name}:
{component|label} is "{HIGH|LOW}";
```

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute dfs_frequency_mode [of]
{module_name|instance_name} [is] {HIGH|LOW};
```

For a more detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name" DFS_FREQUENCY_MODE={LOW|HIGH};
```

where

- LOW, the default, specifies that the frequency of the clock signal at the CLKIN input and at the DFS output clocks (CLKFX and CLKFX180) must fall within the Low frequency range. See *The Programmable Logic Data Book* for the current Low frequency range values for the input clocks (DFS_CLKIN_MIN_LF and DFS_CLKIN_MAX_LF) and for the output clocks (DFS_CLKOUT_MIN_LF and DFS_CLKOUT_MAX_LF).
- HIGH specifies that the frequency of the clock signal at the CLKIN input and at the DFS output clocks (CLKFX and CLKFX180) must fall within the High frequency range. See *The Programmable Logic Data Book* for the current High frequency range values for the input clocks (DFS_CLKIN_MIN_HF and DFS_CLKIN_MAX_HF) and for the output clocks (DFS_CLKOUT_MIN_HF and DFS_CLKOUT_MAX_HF).

The following statement limits the frequency of the clock signal at the CLKIN input and at the DFS output clocks to the High frequency range.

```
INST "foo/bar" DFS_FREQUENCY_MODE=HIGH;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

Directed Routing

Directed Routing Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	No
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

Directed Routing Applicable Elements

Applies only to nets.

Directed Routing Description

Directed Routing is a means of maintaining the routing and timing for a small number of loads and sources. Use of Directed Routing requires that the relative position between the source(s) and load(s) be maintained exactly the same.

Directed Routing Propagation Rules

Not applicable.

Directed Routing Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

The following examples are for illustrative purposes only, and are not valid executables.

It is important to remember that formulation of a Directed Routing constraint requires the placement of the source and load components in a fixed location relative to each other.

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Directed Routing constraints must be generated through the use of the FPGA Editor. To access this capability from within FPGA Editor, click on the **Tools** menu option, then select **Directed Routing Constraints**. (See instructions on the use of the FPGA Editor for further details.)

When you are using the FPGA Editor, you are provided with three choices for the type of Placement Constraint to be generated automatically on the source(s) and load(s) components. Following are examples of responses to each of those settings:

First Setting Option: Do not generate Placement Constraint

This setting will generate a constraint for the routing only. It is designed to be used with existing RPMs.

```
NET "net_name" ROUTE="{2;1;-4!-1;-53320;2920;14;90;200;30;13!0;-2091;1480;24!0;16;-8!}";
```

Second Setting Option: Use Relative Location Constraint

This setting will generate an RPM for the source and load components along with the routing constraint. The RPM can be relocated around the device letting the Placer make the final decision on placement.

```
NET "net_name" ROUTE="{2;1;-4!-1;-53320;2920;14;90;200;30;13!0;-2091;1480;24!0;16;-8!}";
INST "inst1" RLOC=X3Y0;
INST "inst1" RPM_GRID=GRID;
INST "inst1" U_SET=macro name;
INST "inst1" BEL="F";
INST "inst2" RLOC=X3Y0;
INST "inst2" U_SET=macro name;
INST "inst2" BEL="G";
```

Note: In the above example, each RLOC reference signals the launch of a new instance. Hence, there are three instances encompassed within this example.

Third Setting Option: Use Absolute Location Constraint

This setting will cause the source and load components attached to the target net to be locked in place.

```
NET "net_name" ROUTE="{2;1;-4!-1;-53320;2920;14;90;200;30;13!0;-2091;1480;24!0;16;-8!}";
INST "inst1" RLOC=X3Y0;
INST "inst1" RPM_GRID=GRID;
INST "inst1" RLOC_ORIGIN=X87Y200;
INST "inst1" U_SET=macro name;
INST "inst1" BEL="F";
INST "inst2" RLOC=X0Y1;
INST "inst2" U_SET=macro name;
INST "inst2" BEL="F";
INST "inst3" RLOC=X3Y0;
INST "inst3" U_SET=macro name;
INST "inst3" BEL="G";
```

XST Command Line

Not applicable.

Project Navigator

Not applicable.

DISABLE

DISABLE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

DISABLE Applicable Elements

Global in constraints file

DISABLE Description

DISABLE is an advanced timing constraint. It controls path tracing. See also “ENABLE”. All path tracing control statements from any source (netlist, UCF, or NCF) are passed forward to the PCF. It is not possible to override a `DISABLE` in the netlist with an `ENABLE` in the UCF.

DISABLE Propagation Rules

Disables timing analysis of specified block delay symbol.

DISABLE Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

```
DISABLE=delay_symbol_name;
```

where *delay_symbol_name* is the name of one of the standard block delay symbols for path tracing or a specific delay name in the datasheet. These symbols are listed in the following table. Component delay names are also supported in the PCF.

Table 36-1: **Standard Block Delay Symbols for Path Tracing**

Delay Symbol Name	Path Type	Default
reg_sr_q	Asynchronous Set/Reset to output propagation delay	Disabled
reg_sr_clk	Synchronous Set/Reset to clock setup and hold checks	Enabled
lat_d_q	Data to output transparent latch delay	Disabled
ram_we_o	RAM write enable to output propagation delay	Enabled
tbuf_t_o	TBUF 3-state to output propagation delay	Enabled
tbuf_i_o	TBUF input to output propagation delay	Enabled
io_pad_i	IO pad to input propagation delay	Enabled
io_t_pad	IO 3-state to pad propagation delay	Enabled

Table 36-1: **Standard Block Delay Symbols for Path Tracing**

Delay Symbol Name	Path Type	Default
io_o_i	IO output to input propagation delay. Disabled for 3-stated IOBs.	Enabled
io_o_pad	IO output to pad propagation delay.	Enabled

The following statement prevents timing analysis on any path that includes the I to O delay on any TBUF component in the design.

```
DISABLE=tbuf_i_o;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

The syntax is the same as UCF.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

DLL_FREQUENCY_MODE

DLL_FREQUENCY_MODE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

DLL_FREQUENCY_MODE Applicable Elements

DCM (Digital Clock Manager)

DLL_FREQUENCY_MODE Description

DLL_FREQUENCY_MODE is a basic DCM constraint. It specifies the frequency range allowed at the CLKIN input for the DCM's clock delayed locked loop (DLL).

The valid values are LOW and HIGH.

where

- LOW, the default, specifies that the frequency of the clock signal at the CLKIN input and at the DLL output clocks must be in the Low frequency range. See *The Programmable Logic Data Book* for the current Low frequency range values for the input clocks (DLL_CLKIN_MIN_LF and DLL_CLKIN_MAX_LF) and for the output clocks (DLL_CLKOUT_MIN_LF and DLL_CLKOUT_MAX_LF).

- HIGH specifies that the frequency of the clock signal at the CLKIN input and at the DLL output clocks must be in the High frequency range. See *The Programmable Logic Data Book* for the current High frequency range values for the input clocks (DLL_CLKIN_MIN_HF and DLL_CLKIN_MAX_HF) and for the output clocks (DLL_CLKOUT_MIN_HF and DLL_CLKOUT_MAX_HF).

  The CLK90, CLK270, CLK2X, and CLK2X180 outputs are disabled when DLL_FREQUENCY_MODE=HIGH.

DLL_FREQUENCY_MODE Propagation Rules

It is illegal to attach DLL_FREQUENCY_MODE to a net or signal. When attached to a DCM, DLL_FREQUENCY_MODE is propagated to all applicable elements of the DCM.

DLL_FREQUENCY_MODE Syntax Examples

Schematic

Attach to a DCM instance.

Attribute Name—DLL_FREQUENCY_MODE

Attribute Values—LOW, HIGH

VHDL

Before using DLL_FREQUENCY_MODE, declare it with the following syntax:

```
attribute dll_frequency_mode: string;
```

After DLL_FREQUENCY_MODE has been declared, specify the VHDL constraint as follows:

```
attribute dll_frequency_mode of {component_name|label_name}:
{component|label} is "{LOW|HIGH}";
```

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
// synthesis attribute dll_frequency_mode [of]
{module_name|instance_name} [is] {LOW|HIGH};
```

For a more detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name" DLL_FREQUENCY_MODE={LOW|HIGH};
```

The following statement limits the frequency of the clock signal at the CLKIN input and at the DLL output clocks in the High frequency range.

```
INST “foo/bar” DLL_FREQUENCY_MODE=HIGH;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

DRIVE

DRIVE Architecture Support

See the next section, "DRIVE Applicable Elements" for a description of the numerals (1, 2, 3).

Architecture	Supported/Unsupported
Virtex	1, 2, 3
Virtex-E	1, 2, 3
Spartan-II	1, 2, 3
Spartan-IIE	1, 2, 3
Spartan-3	1, 2, 3
Spartan-3E	1, 2, 3
Virtex-II	1, 2, 3
Virtex-II Pro	1, 2, 3
Virtex-II Pro X	1, 2, 3
Virtex-4	1, 2, 3
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

DRIVE Applicable Elements

1. IOB output components (OBUF, OFD, etc.)
2. SelectIO output buffers with IOSTANDARD = LVTTL, LVCMOS15, LVCMOS18, LVCMOS25, or LVCMOS33
3. Nets

DRIVE Description

DRIVE is a basic mapping directive that selects the output for Virtex, Virtex-E, Virtex-II, Virtex-II Pro, Virtex-II Pro X, Virtex-4, Spartan-II, Spartan-IIE, and Spartan-3. DRIVE selects output drive strength (mA) for the SelectIO buffers that use the LVTTL, LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, or LVCMOS33 interface I/O standard.

Note: You cannot change the LVCMOS drive strengths for Virtex-E. Only the variable LVTTL drive strengths are available for Spartan-IIE and Virtex-E.

DRIVE Propagation Rules

DRIVE is illegal when attached to a net or signal, except when the net or signal is connected to a pad. In this case, DRIVE is treated as attached to the pad instance. When attached to a design element, DRIVE is propagated to all applicable elements in the hierarchy below the design element.

DRIVE Syntax Examples

Schematic

Attach to a valid IOB output component.

Attribute Name—DRIVE.

Attribute Values—See the UCF section.

VHDL

Before using DRIVE, declare it with the following syntax:

```
attribute drive: string;
```

After DRIVE has been declared, specify the VHDL constraint as follows:

```
attribute drive of {component_name|entity_name|label_name}:
{component|entity|label} is "value";
```

See the UCF section for valid *values*.

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute drive [of] {module_name|instance_name} [is]
value;
```

See the UCF section for valid *values*.

For a more detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

IOB Output Components (UCF)

For Spartan-II, Spartan-IIE, Spartan-3, Virtex, Virtex-E, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4:

```
INST "instance_name" DRIVE={2|4|6|8|12|16|24};
```

where 12 mA is the default.

SelectIO Output Components (IOBUF_SelectIO, OBUF_SelectIO, and OBUFT_SelectIO)

- For the LVTTL standard with Spartan-II, Spartan-IIE, Spartan-3, Virtex, Virtex-E, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4:

  INST "*instance_name***" DRIVE={2|4|6|8|12|16|24};**

- For the LVCMOS12, LVCMOS15, and LVCMOS18 standards with Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4:

  INST "*instance_name***" DRIVE={2|4|6|8|12|16};**

- For the LVCMOS25 and LVCMOS33 standards with Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4:

  INST "*instance_name***" DRIVE={2|4|6|8|12|16|24};**

  where 12 mA is the default for all architectures.

XCF

```
MODEL "entity_name" drive={2|4|6|8|12|16|24};

BEGIN MODEL "entity_name"
 NET "signal_name" drive={2|4|6|8|12|16|24};
END;
```

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

In the Ports tab grid with I/O Configuration Options checked, click the DRIVE column in the row with the desired output port name and choose a value from the drop down list.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

DROP_SPEC

DROP_SPEC Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

DROP_SPEC Applicable Elements

Timing constraints

DROP_SPEC Description

DROP_SPEC is an advanced timing constraint. It allows you to specify that a timing constraint defined in the input design should be dropped from the analysis. You can use DROP_SPEC when new specifications defined in a constraints file do not directly override all specifications defined in the input design, and some of these input design specifications need to be dropped.

While this timing command is not expected to be used much in an input netlist (or NCF file), it is legal. If defined in an input design DROP_SPEC must be attached to TIMESPEC.

DROP_SPEC Propagation Rules

It is illegal to attach DROP_SPEC to nets or macros. DROP_SPEC removes a specified timing specification.

DROP_SPEC Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

```
TIMESPEC "TSidentifier"=DROP_SPEC;
```

where TS*identifier* is the identifier name used for the timing specification that is to be removed.

The following statement cancels the input design specification TS67.

```
TIMESPEC "TS67"=DROP_SPEC;
```

XCF

Not yet supported.

Constraints Editor

Not applicable.

PCF

```
"TSidentifier" DROP_SPEC;
```

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

DUTY_CYCLE_CORRECTION

DUTY_CYCLE_CORRECTION Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

DUTY_CYCLE_CORRECTION Applicable Elements

- Any CLKDLL, CLKDLLE (Virtex-E only), or CLKDLLHF instance
- A DCM instance

DUTY_CYCLE_CORRECTION Description

DUTY_CYCLE_CORRECTION is a basic DLL / DCM constraint. It corrects the duty cycle of the CLK0, CLK90, CLK180, and CLK270 outputs.

DUTY_CYCLE_CORRECTION Propagation Rules

It is illegal to attach DUTY_CYCLE_CORRECTION to a net or signal. When attached to a DLL / DCM, DUTY_CYCLE_CORRECTION is propagated to all applicable elements of the DLL / DCM.

DUTY_CYCLE_CORRECTION Syntax Examples

Schematic

Attach to a valid instance.

Attribute Name—DUTY_CYCLE_CORRECTION

Attribute Values—TRUE, FALSE

VHDL

Before using DUTY_CYCLE_CORRECTION, declare it with the following syntax:

```
attribute duty_cycle_correction: string;
```

After DUTY_CYCLE_CORRECTION has been declared, specify the VHDL constraint as follows:

```
attribute duty_cycle_correction of {component_name|label_name}:
{component|label} is “true”;
```

For a more detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
 // synthesis attribute duty_cycle_correction [of]
{module_name|instance_name} [is] true;
```

For a more detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST “instance_name” DUTY_CYCLE_CORRECTION={TRUE|FALSE};
```

where

- TRUE, the default, corrects the duty cycle to be a 50_50 duty cycle.
- FALSE does not change the duty cycle.

The following statement specifies a 50_50 duty cycle for foo/bar.

```
INST “foo/bar” DUTY_CYCLE_CORRECTION=TRUE;
```

XCF

```
MODEL “entity_name” duty_cycle_correction={true|false};

BEGIN MODEL “entity_name”
 INST “instance_name”  duty_cycle_correction={true|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

ENABLE

ENABLE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

ENABLE Applicable Elements

Global in constraints file

ENABLE Description

ENABLE is an advanced timing constraint. It controls what types of paths will be analyzed during static timing. See also “DISABLE”.

ENABLE Propagation Rules

Enables timing analysis for specified path delays.

ENABLE Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

ENABLE can be applied only to a global timespec. The path tracing syntax is as follows in the UCF file.

```
ENABLE= delay_symbol_name;
```

where

delay_symbol_name is the name of one of the standard block delay symbols for path tracing symbols shown in the following table, or a specific delay name defined in the datasheet.

Table 41-1: **Standard Block Delay Symbols for Path Tracing**

Delay Symbol Name	Path Type	Default
reg_sr_q	Asynchronous Set/Reset to output propagation delay	Disabled
reg_sr_clk	Synchronous Set/Reset to clock setup and hold checks	Enabled
lat_d_q	Data to output transparent latch delay	Disabled
ram_we_o	RAM write enable to output propagation delay	Enabled
tbuf_t_o	TBUF 3-state to output propagation delay	Enabled
tbuf_i_o	TBUF input to output propagation delay	Enabled
io_pad_i	IO pad to input propagation delay	Enabled
io_t_pad	IO 3-state to pad propagation delay	Enabled
io_o_1	IO output to input propagation delay. Disabled for 3-stated IOBs	Enabled
io_o_pad	IO output to pad propagation delay	Enabled

XCF

Not yet supported.

Constraints Editor

Not applicable.

PCF

ENABLE=*delay_symbol_name*;

or

TIMEGRP *name* **ENABLE=***delay_symbol_name*;

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

ENUM_ENCODING

ENUM_ENCODING Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

ENUM_ENCODING Applicable Elements

ENUM_ENCODING can be applied to a type or signal. Please note that because ENUM_ENCODING must preserve the external design interface, XST ignores the ENUM_ENCODING constraint when it is used on a port.

ENUM_ENCODING Description

ENUM_ENCODING is a synthesis constraint. Use ENUM_ENCODING to apply a specific encoding to a VHDL enumerated type. The constraint value is a string containing space-separated binary codes. You can only specify ENUM_ENCODING as a VHDL constraint on the considered enumerated type.

When describing a finite state machine using an enumerated type for the state register, you may specify a particular encoding scheme with ENUM_ENCODING. In order for this encoding to be actually used by XST, you must also set FSM_ENCODING to **user** for the considered state register.

ENUM_ENCODING Propagation Rules

Applies to the type or signal to which it is attached.

ENUM_ENCODING Syntax Examples

Schematic

Not applicable.

VHDL

You can specify ENUM_ENCODING as a VHDL constraint on the considered enumerated type, as shown in the example below.

```
...
architecture behavior of example is
type statetype is (ST0, ST1, ST2, ST3);
attribute enum_encoding of statetype : type is "001 010 100 111";
signal state1 : statetype;
signal state2 : statetype;
begin
...
```

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
BEGIN MODEL "entity_name"
 NET "signal_name" enum_encoding="string";
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

EQUIVALENT_REGISTER_REMOVAL

EQUIVALENT_REGISTER_REMOVAL Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

EQUIVALENT_REGISTER_REMOVAL Applicable Elements

You can apply EQUIVALENT_REGISTER_REMOVAL globally or to an entity, module, or signal.

EQUIVALENT_REGISTER_REMOVAL Description

EQUIVALENT_REGISTER_REMOVAL is a synthesis constraint. It enables or disables flip-flop optimization related only to the flip-flops described on the RTL level. (Instantiated flip-flops are not removed). Flip-flop optimization includes the removal of equivalent flip-flops for FPGA and CPLDs and flip-flops with constant inputs for CPLDs. This processing increases the fitting success as a result of the logic simplification implied by the flip-flops elimination. Two values are available (**TRUE** and **FALSE** are available in XCF as well):

- **YES** (check box is checked)
  Flip-flop optimization is allowed. This is the default.

- **NO** (check box is not checked)
  Flip-flop optimization is inhibited.

The flip-flop optimization algorithm is time consuming. When fast processing is desired, this option must be invalidated.

EQUIVALENT_REGISTER_REMOVAL Propagation Rules

Removes equivalent flip-flops and flip-flops with constant inputs.

EQUIVALENT_REGISTER_REMOVAL Syntax Examples

Schematic

Not applicable.

VHDL

Before using EQUIVALENT_REGISTER_REMOVAL, declare it with the following syntax:

```
attribute shift_extract: string;
```

After EQUIVALENT_REGISTER_REMOVAL has been declared, specify the VHDL constraint as follows:

```
attribute equivalent_register_removal of {entity_name|signal_name}:
{signal|entity} is “yes”;
```

For a more detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
 // synthesis attribute equivalent_register_removal [of]
{module_name|signal_name} [is] “yes”;
```

For a more detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL “entity_name” equivalent_register_removal={true|false|yes|no};

BEGIN MODEL “entity_name”
 NET “signal_name”  equivalent_register_removal={true|false|yes|no};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-equivalent_register_removal** command line option of the **run** command. Following is the basic syntax:

```
-equivalent_register_removal {YES|NO}
```

The default is **YES**.

Project Navigator

You can define Equivalent Register Removal in the Xilinx Specific Option tab in the Process Properties dialog box within the Project Navigator. The default is **YES** (check box is checked).

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

FAST

FAST Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

FAST Applicable Elements

Output primitives, output pads, bidirectional pads

You can also attach FAST to the net connected to the pad component in a UCF file. NGDBuild transfers the constraint from the net to the pad instance in the NGD file so that it can be processed by the mapper. Use the following syntax:

```
NET "net_name" FAST;
```

FAST Description

FAST is a basic mapping constraint. It increases the speed of an IOB output. FAST produces a faster output but may increase noise and power consumption.

FAST Propagation Rules

FAST is illegal when attached to a net except when the net is connected to a pad. In this instance, FAST is treated as attached to the pad instance. When attached to a macro, module, or entity, FAST is propagated to all applicable elements in the hierarchy below the module.

FAST Syntax Examples

Schematic

Attach to a valid instance.

Attribute Name—FAST

Attribute Values—TRUE, FALSE

VHDL

Before using FAST, declare it with the following syntax:

```
attribute FAST: string;
```

After FAST has been declared, specify the VHDL constraint as follows:

```
attribute FAST of signal_name: signal is “true”;
```

For a more detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute fast [of] signal_name [is] “true”;
```

For a more detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

```
XILINX PROPERTY 'FAST mysignal’;
```

UCF/NCF

The following statement increases the output speed of the element y2:

```
INST “$1I87/y2” FAST;
```

The following statement increases the output speed of the pad to which net1 is connected:

```
NET “net1” FAST;
```

XCF

```
BEGIN MODEL “entity_name”
 NET “signal_name” fast={true|false};
END;
```

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

In the Ports tab grid with I/O Configuration Options checked, click the FAST/SLOW column in the row with the desired output port name and choose FAST from the drop down list.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

FEEDBACK

FEEDBACK Architecture Support

The following table lists supported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

FEEDBACK Applicable Elements

Not applicable.

FEEDBACK Description

FEEDBACK is a constraint that is associated with the DCM. The constraint specifies the external path delay that occurs when a DCM output drives off-chip and then back on-chip into the DCM CLKFB input. This data is required for the timing tools to properly analyze the path clocked for the DCM.

The basic UCF syntax is:

```
NET feedback_signal FEEDBACK = real units NET output_signal;
```

The feedback signal is the net that drives the CLKFB input of the DCM and the output signal is the net that drives the output pad. The *real* value provides the path delay from the output pad to the input pad. If *units* are not specified, then ns is assumed.

FEEDBACK Propagation Rules

Both the *feedback_signal* and *output_signal* must correspond to pad nets. If attached to any other net, an error will result. The *feedback_signal* must be an input pad and *output_signal* must be an output pad.

FEEDBACK Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF

The basic UCF syntax is:

```
NET feedback_signal FEEDBACK =real units NEToutput_signal;
```

feedback_signal is the name of the input pad net used as the feedback to the DCM

real is the board trace delay calculated or measured by you.

units is either ns or ps. The default is ns.

output_signal is the name of the output pad net driven by the DCM.

NCF

Not applicable.

XCF

```
BEGIN MODEL "entity_name"
NETfeedback_signal FEEDBACK = real units NET output_signal;
END;
```

See the UCF section for a description of *_feedback_signal*, *real*, *units*, *output_signal*.

Constraints Editor

Not applicable.

PCF

{**BEL** | **COMP**} *feedback_signal_pad* **FEEDBACK =** *real units* {**BEL** | **COMP**} *output_signal*;

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

FILE

FILE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

FILE Applicable Elements

Instance declaration where the definition is defined in the specified file.

FILE Description

When you instantiate a module that resides in another netlist, ngdbuild finds this file by looking it up by the file name. This requires the netlist to have the same name as module that is defined in the file. If you want to name the netlist differently then the module name, the FILE constraint can be attached to a instance declaration. This tells ngdbuild to look for the module in the file specified.

Please note that in some cases existing Xilinx constraints can not be used in attributes, because they are VHDL key words at the same time. In order to avoid this problem, you may use a constraint alias approach introduced in the 7.1i release. Starting from 7.1 release each constraint has its own alias. The alias name is based on the original constraint name

with a “XIL” prefix. For example, the FILE constraint cannot be used in attributes directly. You have to use “XIL_FILE” instead. The existing XILFILE alias is still supported.

FILE Propagation Rules

Only applicable on instances.

FILE Syntax Examples

Schematic

Attach to a valid instance.

Attribute Name—FILE

Attribute Values—*file_name*.*extension*

where *file_name* is the name of a file that represents the underlying logic for the element carrying the constraint. Example file types include EDIF, EDN, NGC, and NMC.

VHDL

Before using XILFILE, declare it with the following syntax:

```
attribute xilfile: string;
```

After XILFILE has been declared, specify the VHDL constraint as follows:

```
attribute xilfile of {instance_name|component_name} : {label|component}
is “ file_name”;
```

For a more detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute xilfile [of] instance_name is “file_name”;
```

For a more detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

Not applicable.

UCF/NCF

```
INST <instance definition> FILE= <filename definition is located in>;
```

Note: No valid syntax for UCF.

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

FLOAT

FLOAT Architecture Support

The following table lists supported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	No
Spartan-3E	No
Virtex-II	No
Virtex-II Pro	No
Virtex-II Pro X	No
Virtex-4	No
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

FLOAT Applicable Elements

Applies to nets or pins.

FLOAT Description

FLOAT is a basic mapping constraint. It is used to allow 3-stated pads to float when not being driven. This is useful when the default termination for applicable I/Os is set to PULLUP, PULLDOWN, or KEEPER in Project Navigator.

FLOAT Propagation Rules

Applies to the net or pin to which it is attached

FLOAT Syntax Examples

Schematic

Attach to a valid instance.

Attribute Name—FLOAT

Attribute Value— None required. If attached, TRUE is assumed.

VHDL

Before using FLOAT, declare it with the following syntax:

```
attribute FLOAT: string;
```

After FLOAT has been declared, specify the VHDL constraint as follows:

```
attribute FLOAT of signal_name : signal is “TRUE”;
```

Verilog

Specify as follows:

```
// synthesis attribute FLOAT [of] signal_name [is] “TRUE”;
```

ABEL

```
XILINX PROPERTY 'FLOAT signal_name';
```

UCF/NCF

The basic UCF syntax is:

```
NET “signal_name” FLOAT;
```

XCF

```
BEGIN MODEL “entity_name”
   NET "signal_name" FLOAT;
END;
```

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

FROM-THRU-TO

FROM-THRU-TO Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

FROM-THRU-TO Applicable Elements

Predefined and user-defined groups.

FROM-THRU-TO Description

FROM-TO-THRU is an advanced timing constraint, and is associated with the PERIOD constraint of the high or low time. From synchronous paths, a FROM-TO-THRU constraint only controls the setup path, not the hold path. This constraint applies to a specific path that begins at a source group, passes through intermediate points, and ends at a destination group. The source and destination groups can be either user or predefined groups. You must define an intermediate path using TPTHRU before using THRU.

FROM-THRU-TO Propagation Rules

Applies to the specified FROM-THRU-TO path only.

FROM-THRU-TO Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

```
TIMESPEC "TSidentifier"=FROM "source_group" THRU
"thru_pt1"...[THRU"thru_pt2"...] TO "destination_group" value [Units];
```

identifier can consist of characters or underbars.

source_group and *destination_group* are user-defined or predefined groups.

thru_pt1 and *thru_pt2* are intermediate points to define specific paths for timing analysis.

value is the delay time.

units can be ps, ms, ns, or us.

FROM or TO is optional; you can have just a FROM or just a TO.

You are not required to have a FROM, THRU, and TO. You can basically have any combination (FROM-TO, FROM-THRU-TO, THRU-TO, TO, FROM, FROM-THRU-THRU-THRU-TO, FROM-THRU, and so on). There is no restriction on the number of THRU points. The source, thru points, and destination can be a net, bel, comp, macro, pin, or timegroup.

XCF

Not yet supported.

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

1. Identify the through points using the Create ... Timing THRU Points button from the Advanced tab.
2. Set a FROM-THRU-TO constraint for groups of elements in the Advanced tab by clicking Specify next to “Slow / Fast Path Exceptions” (to set explicit times) or Specify next to “Multi Cycle Paths“ (to set times relative to other time specifications).
3. Fill out the FROM / THRU / TO dialog box.

PCF

```
PATH "name"=FROM "source" THRU "thru_pt1" ...THRU "thru_ptn" TO
"destination";
```

You are not required to have a FROM, THRU, and TO. You can basically have any combination (FROM-TO, FROM-THRU-TO, THRU-TO, TO, FROM, FROM-THRU-THRU-THRU-TO, FROM-THRU, and so on). There is no restriction on the number of THRU points. The source, thru points, and destination can be a net, bel, comp, macro, pin, or timegroup.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

FROM-TO

FROM-TO Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

FROM-TO Applicable Elements

Predefined and user-defined groups

FROM-TO Description

FROM-TO defines a timing constraint between two groups, and is associated with the PERIOD constraint of the high or low time. A group can be user-defined or predefined. From synchronous paths, a FROM-TO constraint only controls the setup path, not the hold path.

FROM-TO Propagation Rules

Applies to a path specified between two groups.

FROM-TO Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

```
TIMESPEC "TSname"=FROM "group1" TO "group2" value;
```

TS*name* must always begin with "TS". Any alphanumeric character or underscore may follow.

group1 is the origin path

group2 is the destination path

value in ns by default. Other possible values are MHz or another timing specification such as TS_C2S / 2 or TS_C2S*2.

XCF

Only the basic form of FROM-TO is supported. (Linked Specification and specification using intermediate points are not supported).

But there are some additional limitations:

- FROM without TO and TO without FROM are not supported.

  ```
  TIMESPEC TS_1 = FROM TG1 2 ns;
  ```

  ```
  TIMESPEC TS_1 = TO TG1 2 ns;
  ```

- Pattern matching for predefined groups is not supported:

  ```
  TIMESPEC TS_1 = FROM FFS(machine/*) TO FFS 2 ns;
  ```

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

In the Advanced tab, click Specify next to "Slow / Fast Path Exceptions" (to set explicit times) or Specify next to "Multi Cycle Paths" (to set times relative to other time specifications) and then fill out the FROM / THRU / TO dialog box.

PCF

```
PATH "name"=FROM "group1" TO "group2" value;
```

You are not required to have a FROM, THRU, and TO. You can basically have any combination (FROM-TO, FROM-THRU-TO, THRU-TO, TO, FROM, FROM-THRU-THRU-THRU-TO, FROM-THRU, and so on). There is no restriction on the number of THRU points. The source, thru points, and destination can be a net, bel, comp, macro, pin, or timegroup.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

FSM_ENCODING

FSM_ENCODING Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

FSM_ENCODING Applicable Elements

FSM_ENCODING can be applied globally or to a VHDL entity, Verilog module, or signal.

FSM_ENCODING Description

FSM_ENCODING is a synthesis constraint. It selects the finite state machine coding technique to use. Available property values are **auto, one-hot**, **compact**, **sequential**, **gray**, **johnson**, **speed1**, and **user**. FSM_ENCODING defaults to **auto**, meaning that the best coding technique is automatically selected for each individual state machine.

FSM_ENCODING Propagation Rules

Applies to the entity, module, or signal to which it is attached.

FSM_ENCODING Syntax Examples

Schematic

Not applicable.

VHDL

Before using FSM_ENCODING, declare it with the following syntax:

```
attribute fsm_encoding: string;
```

After FSM_ENCODING has been declared, specify the VHDL constraint as follows:

```
attribute fsm_encoding of {entity_name|signal_name}: {entity|signal} is
"{auto|one-hot|compact|gray|sequential|johnson|speed1|user}";
```

The default is **AUTO**.

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute fsm_encoding [of] {module_name|signal_name}
[is] {auto|one-hot|compact|gray|sequential|johnson|speed1|user};
```

The default is **AUTO**.

For a more detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL "entity_name" fsm_encoding={auto|one-
hot|compact|sequential|gray|johnson|speed1|user};


BEGIN MODEL "entity_name"
 NET "signal_name" fsm_encoding={auto|one-
 hot|compact|sequential|gray|johnson|speed1|user};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-fsm_encoding** command line option of the **run** command. Following is the basic syntax:

```
-fsm_encoding {Auto|One-
Hot|Compact|Sequential|Gray|Johnson|Speed1|User}
```

The default is **AUTO**.

Project Navigator

From the Project Navigator point of view, the -fsm_encoding option is coupled with -fsm_extract. These 2 options are represented by a single menu—FSM Encoding Algorithm:

- If the FSM Encoding Algorithm menu is None, then -fsm_extract is set to No and the -fsm_encoding option has no influence on the synthesis.
- In all other cases, -fsm_extract is set to Yes and -fsm_encoding is set to the value selected in the menu.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the HDL Options tab of the Process Properties dialog box. Select a value from the drop-down list box.

FSM_EXTRACT

FSM_EXTRACT Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

FSM_EXTRACT Applicable Elements

FSM_EXTRACT can be applied globally or to a VHDL entity, Verilog module or signal.

FSM_EXTRACT Description

FSM_EXTRACT is a synthesis constraint. It enables or disables finite state machine extraction and specific synthesis optimizations. Allowed values are YES and NO (TRUE and FALSE ones are available in XCF as well).

By default, FSM synthesis is enabled (**YES**). This option must be enabled in order to set values for the FSM Encoding Algorithm and FSM Flip-Flop Type.

FSM_EXTRACT Propagation Rules

Applies to the entity, module, or signal to which it is attached.

FSM_EXTRACT Syntax Examples

Schematic

Not applicable.

VHDL

Before using FSM_EXTRACT, declare it with the following syntax:

```
attribute fsm_extract: string;
```

After FSM_EXTRACT has been declared, specify the VHDL constraint as follows:

```
attribute fsm_extract of {entity_name|signal_name}: {entity|signal} is
“yes”;
```

For a more detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
 // synthesis attribute fsm_extract [of] {module_name|signal_name} [is]
yes;
```

For a more detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL “entity_name” fsm_extract={yes|no|true|false};


BEGIN MODEL “entity_name”
 NET “signal_name” fsm_extract={yes|no|true|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-fsm_extract** command line option of the **run** command. Following is the basic syntax:

```
-fsm_extract {YES|NO}
```

The default is **YES**.

Project Navigator

In terms of the Project Navigator, the -fsm_extract option is coupled with -fsm_encoding. These two options are represented by a single menu: FSM Encoding Algorithm.

- If the FSM Encoding Algorithm menu is None, then -fsm_extract is set to **no** and the -fsm_encoding option has no influence on the synthesis.
- In all other cases, -fsm_extract is set to **yes** and -fsm_encoding is set to the value selected in the menu.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the HDL Options tab of the Process Properties dialog box. Select a value from the drop-down list box.

FSM_STYLE

FSM_STYLE Architecture Support

The following table lists supported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

FSM_STYLE Applicable Elements

FSM_STYLE can be applied globally or to a VHDL entity, Verilog module, or signal

FSM_STYLE Description

This constraint directs the Synthesis tool to map Finite State Machines (FSMs) either in Look-Up Tables (LUTs) or BlockRAM (BRAM). It is both a global and a local constraint.

FSM_STYLE Propagation Rules

Applies to the entity, module, or signal to which it is attached.

FSM_STYLE Syntax Examples

Schematic

Not applicable

VHDL

Before using FSM_STYLE, declare it with the following syntax:

```
attribute fsm_style: string;
```

After FSM_STYLE has been declared, specify the VHDL constraint as follows:

```
attribute fsm_style of {entity_name|signal_name}: {entity|signal} is
"{lut|bram}";
```

The default is **lut**.

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute FSM_STYLE [of]
{module_name|instance_name|signal_name} [is] {lut|bram};
```

For a more detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name" FSM_STYLE={lut|bram};
```

XCF

```
MODEL "entity_name" FSM_STYLE = {lut|bram};

BEGIN MODEL "entity_name"
 INST "instance_name" FSM_STYLE = {lut|bram};
 NET "net_name" FSM_STYLE = {lut|bram};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

FULL_CASE

FULL_CASE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

FULL_CASE Applicable Elements

You can apply FULL_CASE to case statements in Verilog meta comments only.

FULL_CASE Description

The **full_case** directive is an XST synthesis constraint.

FULL_CASE Propagation Rules

Not applicable.

FULL_CASE Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

The directive is exclusively available as a meta comment in your Verilog code and cannot be specified in a VHDL description or in a separate constraint file. The syntax differs from the standard meta comment syntax as shown in the following:

```
// synthesis full_case
```

The Verilog 2001 syntax is as follows: (* full_case *)

Since the directive does not contain a target reference, the meta comment immediately follows the selector.

Example:

```
casex select // synthesis full_case or ( * full_case *)
4'b1xxx: res = data1;
4'bx1xx: res = data2;
4'bxx1x: res = data3;
4'bxxx1: res = data4;
endcase
```

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define FULL_CASE globally with the -vlgcase command line option of the run command. Following is the basic syntax:

```
-vlgcase {full|parallel|full-parallel}
```

Project Navigator

For Verilog files only, you can specify FULL_CASE globally in the Synthesis Options tab of the Process Properties dialog box within the Project Navigator.

With a Verilog design selected in the Sources window, right-click Synthesize in the Processes window to access the Synthesis Options tab of the Process Properties dialog box. For Case Implementation Style, select Full as a Value.

HBLKNM

HBLKNM Architecture Support

Note: The numbers in the second column indicate applicable elements. See the HBLKNM Applicable Elements section (following).

Architecture	Supported/Unsupported
Virtex	1, 2, 3, 5, 6, 8, 9, 10, 11
Virtex-E	1, 2, 3, 5, 6, 7, 8, 9, 10, 11
Spartan-II	1, 2, 3, 5, 6, 8, 9, 10, 11
Spartan-IIE	1, 2, 3, 5, 6, 7, 8, 9, 10, 11
Spartan-3	1, 2, 3, 5, 6, 8, 9, 10, 11
Spartan-3E	1, 2, 3, 5, 6, 8, 9, 10, 11
Virtex-II	1, 2, 3, 5, 6, 8, 9, 10, 11
Virtex-II Pro	1, 2, 3, 5, 6, 8, 9, 10, 11
Virtex-II Pro X	1, 2, 3, 5, 6, 8, 9, 10, 11
Virtex-4	1, 2, 3, 5, 6, 8, 9, 10, 11
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

HBLKNM Applicable Elements

1. Registers
2. I/O elements and pads
3. FMAP
4. BUFT
5. PULLUP
6. ACLK, GCLK
7. BUFG
8. BUFGS, BUFGP
9. ROM
10. RAMS and RAMD
11. Carry logic primitives

You can also attach HBLKNM to the net connected to the pad component in a UCF file. NGDBuild transfers the constraint from the net to the pad instance in the NGD file so that it can be processed by the mapper. Use the following syntax:

```
NET "net_name" HBLKNM=property_value;
```

HBLKNM Description

HBLKNM is an advanced mapping constraint. It assigns hierarchical block names to logic elements and controls grouping in a flattened hierarchical design. When elements on different levels of a hierarchical design carry the same block name and the design is flattened, NGDBuild prefixes a hierarchical path name to the HBLKNM value.

Like BLKNM, HBLKNM forces function generators and flip-flops into the same CLB. Symbols with the same HBLKNM constraint map into the same CLB, if possible.

However, using HBLKNM instead of BLKNM has the advantage of adding hierarchy path names during translation, and therefore the same HBLKNM constraint and value can be used on elements within different instances of the same design element.

HBLKNM Propagation Rules

When attached to a design element, HBLKNM is propagated to all applicable elements in the hierarchy within the design element.

HBLKNM Syntax Examples

Schematic

Attach to a valid instance.

Attribute Name—HBLKNM

Attribute Values—*block_name*

VHDL

Before using HBLKNM, declare it with the following syntax:

```
attribute hblkmnm: string;
```

After HBLKNM has been declared, specify the VHDL constraint as follows:

```
attribute hblknm of
{entity_name|component_name|signal_name|label_name}:
{entity|component|signal|label} is "block_name";
```

where *block_name* is a valid block name for that type of symbol.

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute hblknm [of]
{module_name|instance_name|signal_name} [is] block_name;
```

where *block_name* is a valid block name for that type of symbol.

For a more detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
NET “net_name” HBLKNM=property_value;
INST “instance_name” HBLKNM=block_name;
```

where *block_name* is a valid block name for that type of symbol.

The following statement specifies that the element this_fmap will be put into the block named group1.

```
INST “$I13245/this_fmap” HBLKNM=group1;
```

The following statement attaches HBLKNM to the pad connected to net1.

```
NET “net1” HBLKNM=$COMP_0;
```

Elements with the same HBLKNM are placed in the same logic block if possible. Otherwise an error occurs. Conversely, elements with different block names will not be put into the same block.

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

HIGH_FREQUENCY

HIGH_FREQUENCY Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

HIGH_FREQUENCY Applicable Elements

DLL

HIGH_FREQUENCY Description

HIGH_FREQUENCY is a basic DLL constraint. It specifies the frequency range allowed at the CLKIN input for the DLL's clock delayed locked loop (DLL).

HIGH_FREQUENCY Propagation Rules

It is illegal to attach HIGH_FREQUENCY to a net or signal. When attached to a DLL, HIGH_FREQUENCY is propagated to all applicable elements of the DLL.

HIGH_FREQUENCY Syntax Examples

Schematic

Attach to a DCM instance.

Attribute Name—HIGH_FREQUENCY

Attribute Values—LOW, HIGH

VHDL

Before using HIGH_FREQUENCY, declare it with the following syntax:

```
attribute high_frequency: string;
```

After HIGH_FREQUENCY has been declared, specify the VHDL constraint as follows:

```
attribute high_frequency of {component_name|label_name}:
{component|label} is "{LOW|HIGH}";
```

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
// synthesis attribute high_frequency [of] {module_name|instance_name}
[is] {LOW|HIGH};
```

For a more detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name" HIGH_FREQUENCY={LOW|HIGH};
```

where

- LOW, the default, specifies that the frequency of the clock signal at the CLKIN input and at the DLL output clocks must be in the Low frequency range. See *The Programmable Logic Data Book* for the current Low frequency range values for the input clocks (DLL_CLKIN_MIN_LF and DLL_CLKIN_MAX_LF) and for the output clocks (DLL_CLKOUT_MIN_LF and DLL_CLKOUT_MAX_LF).
- HIGH specifies that the frequency of the clock signal at the CLKIN input and at the DLL output clocks must be in the High frequency range. See *The Programmable Logic Data Book* for the current High frequency range values for the input clocks (DLL_CLKIN_MIN_HF and DLL_CLKIN_MAX_HF) and for the output clocks (DLL_CLKOUT_MIN_HF and DLL_CLKOUT_MAX_HF).

  The CLK90, CLK270, CLK2X, and CLK2X180 outputs are disabled when HIGH_FREQUENCY=HIGH.

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

HU_SET

HU_SET Architecture Support

Note: The numbers in the second column indicate applicable elements. See the HU_SET Applicable Elements section (following).

Architecture	Supported/Unsupported
Virtex	1, 2, 3, 4, 5, 6, 8
Virtex-E	1, 2, 3, 4, 5, 6, 8
Spartan-II	1, 2, 3, 4, 5, 6, 8
Spartan-IIE	1, 2, 3, 4, 5, 6, 8
Spartan-3	1, 2, 3, 4, 5, 7, 9
Spartan-3E	1, 2, 3, 4, 5, 7, 9
Virtex-II	1, 2, 3, 4, 5, 6, 7, 9
Virtex-II Pro	1, 2, 3, 4, 5, 6, 7, 9
Virtex-II Pro X	1, 2, 3, 4, 5, 6, 7, 9
Virtex-4	1, 2, 3, 4, 5, 10, 11
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

HU_SET Applicable Elements

1. Registers
2. FMAP
3. Macro Instance
4. ROM
5. RAMS, RAMD
6. BUFT
7. MULT18X18S
8. RAMB4_Sm_Sn, RAMB4_Sn
9. RAMB16_Sm_Sn, RAMB16_Sn
10. RAMB16
11. DSP48

HU_SET Description

HU_SET is an advanced mapping constraint. It is defined by the design hierarchy. However, it also allows you to specify a set name. It is possible to have only one H_SET within a given hierarchical element but by specifying set names, you can specify several HU_SET sets.

NGDBuild hierarchically qualifies the name of the HU_SET as it flattens the design and attaches the hierarchical names as prefixes.

The differences between an HU_SET constraint and an H_SET constraint include:

HU_SET	H_SET
Has an explicit user-defined and hierarchically qualified name for the set	Has only an implicit hierarchically qualified name generated by the design-flattening program
"Starts" with the symbols that are assigned the HU_SET constrain	"Starts" with the instantiating macro one level above the symbols with the RLOC constraints

For background information about using the various set attributes, see "RLOC Description".

HU_SET Propagation Rules

HU_SET is a design element constraint and any attachment to a net is illegal.

HU_SET Syntax Examples

Schematic

Attach to a valid instance.

Attribute Name—HU_SET

Attribute Values—*set_name*

VHDL

Before using HU_SET, declare it with the following syntax:

```
attribute hu_set: string;
```

After HU_SET has been declared, specify the VHDL constraint as follows:

```
attribute hu_set of {component_name|entity_name|label_name}:
{component|entity|label} is "set_name";
```

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute hu_set [of] {module_name|instance_name} [is]
set_name;
```

For a more detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST “instance_name” HU_SET=set_name;
```

where *set_name* is the identifier for the set.

The variable *set_name* must be unique among all the sets in the design.

The following statement assigns an instance of the register FF_1 to a set named heavy_set.

```
INST “$1I3245/FF_1” HU_SET=heavy_set;
```

XCF

```
MODEL “entity_name” hu_set={yes|no};

BEGIN MODEL “entity_name”
 INST "instance_name" hu_set=yes;
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

INCREMENTAL_SYNTHESIS

INCREMENTAL_SYNTHESIS Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

INCREMENTAL_SYNTHESIS Applicable Elements

INCREMENTAL_SYNTHESIS can be applied globally or to a VHDL entity or Verilog module.

INCREMENTAL_SYNTHESIS Description

The following section discuss Incremental Synthesis Flow, INCREMENTAL_SYNTHESIS, and RESYNTHESIZE.

Incremental Synthesis Flow

The main goal of Incremental Synthesis flow is to reduce the overall time that the designer spends in completing a project. This can be achieved by allowing you to re-synthesize only the modified portions of the design instead of the entire design. We may consider two main categories of incremental synthesis:

- Block Level: The synthesis tool re-synthesizes the entire block if at least one modification was made inside this block.
- Gate or LUT Level: The synthesis tool tries to identify the exact changes made in the design and generates the final netlist with minimal changes.

XST supports block level incremental synthesis with some limitations.

Incremental Synthesis is implemented using two constraints: INCREMENTAL_SYNTHESIS, and RESYNTHESIZE.

INCREMENTAL_SYNTHESIS

Use the INCREMENTAL_SYNTHESIS constraint to control the decomposition of the design on several logic groups.

- If this constraint is applied to a specific block, this block with all its descendents are considered as one logic group, until the next INCREMENTAL_SYNTHESIS constraint is found. During synthesis, XST generates a single NGC file for the logic group.
- Beginning in release 7.1i, you can apply the INCREMENTAL_SYNTHESIS constraint to a block that is instantiated a multiple number of times.

  If a single block is changed, then the entire group is resynthesized and a new NGC file(s) is generated.

  - Beginning in release 7.1i, XST can propagate INCREMENTAL_SYNTHESIS constraints to the NGC netlist in the form of the rangeless area groups. This enables automatic floorplanning in the implementation flow. You can do this by setting the Enable Auto Floorplanning option to *incremental design* under the “Synthesis Options” tab of the Process Properties dialog box. Please note that by default XST does not propagate INCREMENTAL_SYNTHESIS constraints to the final netlist.

Figure 62.1 shows how blocks are grouped by use of the INCREMENTAL_SYNTHESIS constraint.

Consider the following:

- LEVA, LEVA_1, LEVA_2, my_add, my_sub as one logic group
- LEVB, my_and, my_or and my_sub as another logic group
- Top is considered separately as a logic group

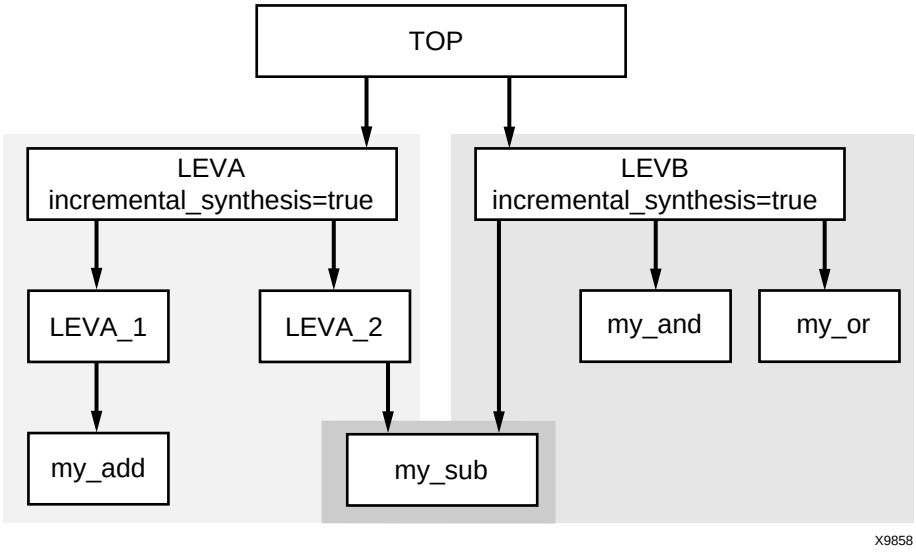


Figure 57-1: **Grouping Through Incremental Synthesis**

RESYNTHESIZE

For VHDL, XST is able to automatically recognize what blocks were changed and to resynthesize only changed ones. This detection is done at the file level. This means that if a VHDL file contains two blocks, both blocks are considered modified. If these two blocks belong to the same logic group, then there is no impact on the overall synthesis time. If the VHDL file contains two blocks that belong to different logic groups, both logic groups are considered changed and so are resynthesized. Xilinx recommends that you only keep different blocks in a single VHDL file if they belong to the same logic group.

Use the RESYNTHESIZE constraint to force resynthesis of the blocks that were not changed.

Note: In the current release, XST runs HDL synthesis on the entire design. However, during low level optimization XST reoptimizes modified blocks only.

In this example, XST generates 3 NGC files as shown in the following log file segment:.

```
...
*
*                  Final Report
*
=========================================================================


 Final Results
 Top Level Output File Name         : c:\users\incr_synt\new.ngc
 Output File Name                   : c:\users\incr_synt\leva.ngc
 Output File Name                   : c:\users\incr_synt\levb.ngc

=========================================================================
 ...
```

If you made changes to the LEVA_1 block, XST automatically resynthesizes the entire logic group, including LEVA, LEVA_1, LEVA_2, my_add, my_sub as shown in the following log file segment.

```
...
=========================================================================
*
*                  Low Level Synthesis
*
=========================================================================


 Final Results
 Incremental synthesis        Unit <my_and> is up to date ...
 Incremental synthesis        Unit <my_and> is up to date ...
 Incremental synthesis        Unit <my_and> is up to date ...
 Incremental synthesis        Unit <my_and> is up to date ...

Optimizing unit <my_sub> ...
Optimizing unit <my_add> ...
Optimizing unit <leva_1> ...
Optimizing unit <leva_2> ...
Optimizing unit <leva> ...

=========================================================================
 ...
```

If you make no changes to the design XST, during Low Level synthesis, reports that all blocks are up to date and the previously generated NGC files are kept unchanged as shown in the following log file segment.

```
...
=========================================================================
*
*                  Low Level Synthesis
*
=========================================================================


 Incremental synthesis: Unit <my_and> is up to date ...
 Incremental synthesis: Unit <my_or> is up to date ...
 Incremental synthesis: Unit <my_sub> is up to date ...
 Incremental synthesis: Unit <my_add> is up to date ...
 Incremental synthesis: Unit <levb> is up to date ...
 Incremental synthesis: Unit <leva_1> is up to date ...
 Incremental synthesis: Unit <leva_2> is up to date ...
 Incremental synthesis: Unit <leva> is up to date ...
 Incremental synthesis: Unit <top> is up to date ...

=========================================================================
 ...
```

If you changed one timing constraint, then XST cannot detect this modification. To force XST to resynthesized the required blocks, use the RESYNTHESIZE constraint. For example, if LEVA must be resynthesized, then apply the RESYNTHESIZE constraint to this block. All blocks included in the <leva> group are reoptimized and a new NGC file is generated as shown in the following log file segment.

```
...
=========================================================================
*
*                  Low Level Synthesis
*
=========================================================================


 Incremental synthesis: Unit <my_and> is up to date ...
 Incremental synthesis: Unit <my_or> is up to date ...
 Incremental synthesis: Unit <levb> is up to date ...
 Incremental synthesis: Unit <top> is up to date ...
...
 Optimizing unit <my_sub> ...
 Optimizing unit <my_add> ...
 Optimizing unit <leva_1> ...
 Optimizing unit <leva_2> ...
 Optimizing unit <leva> ...

=========================================================================
 ...
```

If you have previously run XST in non-incremental mode and then switched to incremental mode or the decomposition of the design was changed, then you must delete all previously generated NGC files before continuing. Otherwise XST issues an error.

If in the previous example, you were to add "incremental_synthesis=true" to the block LEVA_1, then XST displays the following error:

```
ERROR:Xst:624 - Could not find instance <inst_leva_1> of cell <leva_1>
in <leva>
```

The problem most likely occurred because the design was previously run in non-incremental synthesis mode. To fix the problem, remove the existing NGC files from the project directory.

Please note that if you modified the HDL in the top-level block of the design, and at the same time changed the name of the top-level block, XST cannot detect design modifications and resynthesize the top-level block. Force resynthesis by using RESYNTHESIS constraint.

INCREMENTAL_SYNTHESIS Propagation Rules

Applies to the entity or module to which it is attached.

INCREMENTAL_SYNTHESIS Syntax Examples

Schematic

Not applicable.

VHDL

Before using INCREMENTAL_SYNTHESIS, declare it with the following syntax:

```
attribute incremental_synthesis: string;
```

After INCREMENTAL_SYNTHESIS has been declared, specify the VHDL constraint as follows:

```
attribute incremental_synthesis of entity_name: entity is "yes";
```

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
// synthesis attribute incremental_synthesis [of] module_name [is]
"yes";
```

For a more detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL "entity_name" incremental_synthesis={yes|no|true|false};
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Beginning from release 7.1i, XST can propagate INCREMENTAL_SYNTHESIS constraints to the NGC netlist in the form of the rangless area groups. This enables automatic floorplanning in the implementation flow. You can do this by setting the Enable Auto Floorplanning option to *incremental design* under the “Synthesis Options” tab of the Process Properties dialog box. Please note that by default XST does not propagate INCREMENTAL_SYNTHESIS constraints to the final netlist.

INIT

INIT Architecture Support

Note: The numbers in the second column indicate applicable elements. See the INIT Applicable Elements section (following).

Architecture	Supported/Unsupported
Virtex	1, 2, 3
Virtex-E	1, 2, 3
Spartan-II	1, 2, 3
Spartan-IIE	1, 2, 3
Spartan-3	1, 2, 3, 4
Spartan-3E	1, 2, 3
Virtex-II	1, 2, 3, 4
Virtex-II Pro	1, 2, 3, 4
Virtex-II Pro X	1, 2, 3, 4
Virtex-4	1, 2, 3
XC9500, XC9500XL, XC9500XV	2
CoolRunner XPLA3	2
CoolRunner-II	2

INIT Applicable Elements

1. ROM
2. Registers
3. LUTs, SRLs
4. RAMB16_Sn (single-port block RAM)

INIT Description

INIT is a basic initialization constraint. It initializes ROMs, RAMs, registers, and look-up tables. The least significant bit of the value corresponds to the value loaded into the lowest address of the memory element. For register initialization, S indicates Set and R indicates Reset.

You can use INIT to specify the initial value directly on the symbol with the following limitation. INIT may only be used on a ROM that is 1 bit wide and not more than 32 bits deep.

INIT has an additional use with Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X single-port RAMB16s. In Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X, you can initialize each bit in the output register at power-on to either a 0 or a 1. INIT sets the output register value at power on.

INIT Propagation Rules

It is illegal to attach INIT to a net or signal in FPGAs. For CPLDs, you can attach INIT to a net or signal driven by a register, or to a pad-net driven by a register through an output buffer. When attached to a design element, INIT propagates to all applicable elements in the hierarchy below the design element.

Following is a discussion of some example propagations with flip-flops and INITs attached to a signal, port, or bus. The attribute is propagated to the right flip-flop.

Example 1:

If you attach an INIT attribute on a signal, the flip-flop takes the INIT value of the signal or port.

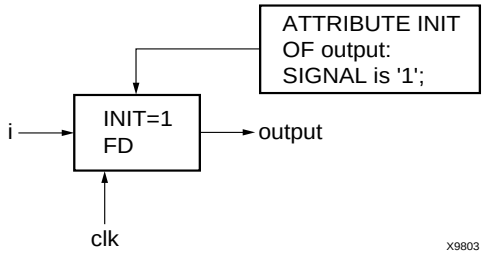


Figure 58-1: **INIT Attribute on a Signal**

Example 2:

If you attach an INIT attribute to a bus, each flip-flop takes the correct INIT value.

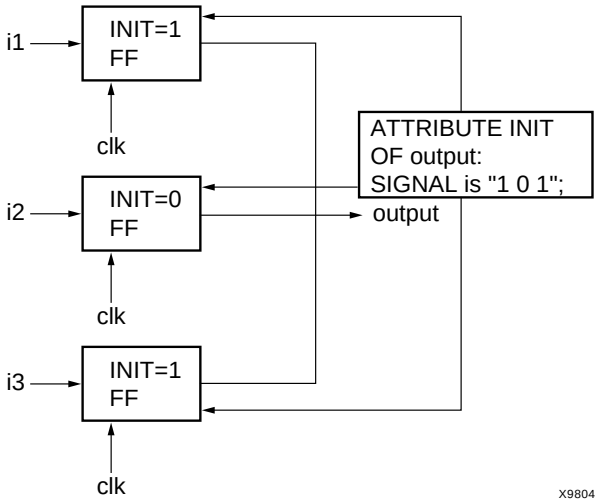


Figure 58-2: **INIT Attribute Attached to a Bus**

Example 3:

One more specific case is the synchronous output enable that infers 2 flip-flops. If you attach an INIT attribute to the signal or port, both flip-flops must be initialized.

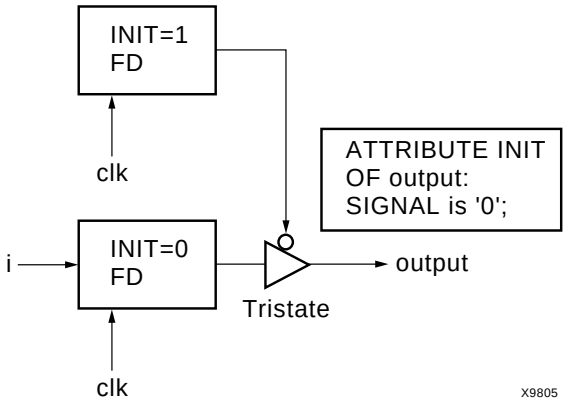


Figure 58-3: **Synchronous Output Enable that Infers Two Flip-Flops**

INIT Syntax Examples

Schematic

Attach to a net, pin, or instance.

Attribute Name—INIT.

Attribute Values—See "INIT Propagation Rules".

VHDL

Before using INIT, declare it with the following syntax:

```
attribute init: string;
```

After INIT has been declared, specify the VHDL constraint as follows:

```
attribute init of {component_name|label_name|signal_name}:
{component|label|signal} is "value";
```

For CPLDs only, use the following syntax:

```
attribute init of signal_name: signal is "{S|R}";
```

See "INIT Propagation Rules" for a description of valid values.

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows for implementation purposes:

```
 // synthesis attribute init [of]
{module_name|instance_name|signal_name} [is] value;
```

For CPLDs only, use the following syntax:

```
// synthesis attribute init [of] signal_name [is] "{S|R}";
```

See "INIT Propagation Rules" for a description of valid values.

For a more detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

```
XILINX PROPERTY 'init={s|r} mysignal';
```

UCF/NCF

This section shows the basic syntax for adding to a UCF design.

For ROM, Registers, LUTs, SRLs

```
INST "instance_name" INIT={value | 1 | 0 | S | R};
```

where *value* is a 4-digit or 8-digit hexadecimal number that defines the initialization string for the memory element, depending on whether the element is 16-bit or 32-bit.

For example, INIT=ABAC1234. If you do not specify INIT, the RAM initializes with zero.

Values	Virtex and Spartan-II
lower INIT values	mapped to the G function generator
upper INIT values	mapped to the F function generator

1 (or S) indicates Set and 0 (or R) indicates Reset for registers.

For Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X RAMB16_Sn

```
INST "instance_name" INIT={1 | 0 | value};
```

where *value* is a hexadecimal number that defines the initialization string for the output register, depending on the width of the RAMB16 port.

For every 4-bits, one hexadecimal value (0 through F) can be entered.

For those ports that include parity bits, the INIT value specifies the parity portion of the output register in the high order bit position, followed by the data portion. For example, to initialize data to zero and parity to one, you would set INIT to "100" for a 9-bit port, to "30000" for an 18-bit port, and to "F00000000" for a 36-bit port.

If INIT is not specified, the RAMB16 output register is initialized with zeros.

XCF

Not applicable.

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

In the Misc tab, click Block RAM, SRL16, ROM, or FFS/LATCH.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

With a design loaded into the Editor, select a component from the List1 dialog box. Click **editblock** and then click **editmode**. The INIT selection boxes are then displayed in the schematic in the main window. Select the Begin Editing icon from the toolbar.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

INIT_A

INIT_A Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

INIT_A Applicable Elements

Port A of RAMB16_Sm_Sn (dual-port block RAM).

INIT_A Description

INIT_A is a basic initialization constraint. It initializes the Port A (Sm) outputs for dual-port RAMB16 components. In Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4, each bit in the output register can be initialized at power-on to either a 0 or a 1. The INIT_A property sets the output register value at power on.

INIT_A Propagation Rules

It is illegal to attach INIT_A to a net or signal. When attached to a macro, module, or entity, INIT_A propagates to all applicable elements in the hierarchy below the macro, module, or entity.

INIT_A Syntax Examples

Schematic

Attach to a logical symbol.

Attribute Name—INIT_A

Attribute Values—*value*

VHDL

Before using INIT_A, declare it with the following syntax:

```
attribute init_a: string;
```

After INIT_A has been declared, specify the VHDL constraint as follows:

```
attribute init_a of {component_name|label_name}: {component|label} is
"value";
```

See the UCF section for a description of *value*.

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute init_a [of] {module_name|instance_name} [is]
value;
```

See the UCF section for a description of *value*.

For a more detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name" INIT_A=value;
```

where *value* is a hexadecimal number that defines the initialization string for the output register, depending on the width of port A. For every 4-bits, one hexadecimal value (0 through F) can be entered.

For those ports that include parity bits, the INIT_A value specifies the parity portion of the output register in the high order bit position, followed by the data portion. For example, to initialize data to zero and parity to one, you would set INIT_A to "100" for a 9-bit port, to "30000" for an 18-bit port, and to "F00000000" for a 36-bit port.

If the INIT_A constraint is not specified, the port A output register is initialized with zeros.

The following statement specifies that the 2 bits of the port A output register of an RAMB16_S2_S9 be set to 100 upon power on.

```
INST "foo/bar" INIT_A=100;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

INIT_B

INIT_B Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

INIT_B Applicable Elements

Port B of RAMB16_Sm_Sn (dual-port block RAM).

INIT_B Description

INIT_B is a basic initialization constraint. It initializes the Port B (Sn) outputs for dual-port RAMB16 components. In Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4, each bit in the output register can be initialized at power-on to either a 0 or a 1. The INIT_B property sets the output register value at power on.

INIT_B Propagation Rules

It is illegal to attach INIT_B to a net or signal. When attached to a design element, INIT_B propagates to all applicable elements in the hierarchy within the design element.

INIT_B Syntax Examples

Schematic

Attach to a logic symbol. See the UCF section.

Attribute Name—INIT_B

Attribute Values—*value*

VHDL

Before using INIT_B, declare it with the following syntax:

```
attribute init_b: string;
```

After INIT_B has been declared, specify the VHDL constraint as follows:

```
attribute init_b of {component_name|label_name}: {component|label} is
"value";
```

See the UCF section for a description of *value*.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute init_b [of] {module_name|instance_name} [is]
value;
```

See the UCF section for a description of *value*.

For a detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name" INIT_B=value;
```

where *value* is a hexadecimal number that defines the initialization string for the output register, depending on the width of port A. For every 4-bits, you can enter one hexadecimal value (0 through F).

For those ports that include parity bits, the INIT_B value specifies the parity portion of the output register in the high order bit position, followed by the data portion. For example, to initialize data to zero and parity to one, you would set INIT_B to "100" for a 9-bit port, to "30000" for an 18-bit port, and to "F00000000" for a 36-bit port.

If the INIT_B constraint is not specified, the port B output register is initialized with zeros.

The following statement specifies that the 9 bits of the port B output register of an RAMB16_S2_S9 be set to 100 upon power on.

```
INST "foo/bar" INIT_B=100;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

INIT_*xx*

INIT_*xx* Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

INIT_*xx* Applicable Elements

- RAMB4_S*n* and RAMB4_S*m*_S*n* components for Spartan-II, Spartan-IIE, Spartan-3, Virtex, Virtex-II, Virtex-E, Virtex-II Pro, Virtex-II Pro X, and Virtex-4
- RAMB16_S*n* and RAMB16_S*m*_S*n* components for Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X only
- RAM16X2S, RAM16X4S, RAM16X8S, RAM32X2S, RAM32X4S, RAM32X8S, RAM64X2S (wide, static, synchronous RAM) for Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X only

INIT_*xx* Description

INIT_*xx* is a basic initialization constraint.

- INIT_00 through INIT_0F specify initialization strings for RAMB4_S*n* and RAMB4_S*m*_S*n* components.

- INIT_00 through INIT_3F specify initialization strings for data memory in RAMB16_Sn and RAMB16_S*m*_S*n* components.
- INIT_00 through INIT_07 specify initialization strings for Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X wide, static, synchronous, RAMs (RAM16X2S, RAM16X4S, for example).

INIT_*xx* Propagation Rules

It is illegal to attach INIT_*xx* to a net, signal, entity, module, or macro.

INIT_*xx* Syntax Examples

Schematic

Attach to a block RAM instance.

Attribute Name—INIT_*xx*.

Attribute Values—*value*.

See the UCF section.

VHDL

Before using INIT_xx, declare it with the following syntax:

```
attribute init_xx: string;
```

After INIT_xx has been declared, specify the VHDL constraint as follows:

```
attribute init_xx of {component_name|label_name}: {component|label} is
"value";
```

For a discussion of *value*, see the UCF section.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute init_xx [of] {module_name|instance_name} [is]
value;
```

For a discussion of *value*, see the UCF section.

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name" INIT_xx=value;
```

where

- For RAMB4s, *xx* a is a two-digit hexadecimal value 00 through 0F that specifies which 256 bits (see Table 61-1) of the 4096-bit data memory to initialize to the specified value.
- For RAMB16s, *xx* is a two-digit hexadecimal value 00 through 3F that specifies which 256 bits (see Table 61-2) of the 16384-bit data memory to initialize to the specified value.
- For Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X, Wide, Static, Synchronous RAM, *xx* a is a two-digit hexadecimal value 00 through 07 that specifies the output port (O0 through O7) whose corresponding RAM cells should be initialized to the specified value.
- *value* is a string of hexadecimal characters up to 64 digits wide. If INIT_*xx* has a value less than the required 64 hex digits, the value will be padded with zeros from the most significant bit (MSB) side. This fills the 256 bits in the initialization string (4 bits per hexadecimal character * 64 characters).

Table 61-1: **RAMB4 INIT_xx Data Memory Addresses**

INIT_*xx*	**RAMB4 Addresses**				
	4096 x 1	**2048 x 2**	**1024 x 4**	**512 x 8**	**256 x 16**
INIT_00	255 -- 0	127 - 0	63 - 0	31 - 0	15 - 0
INIT_01	511 - 256	255 - 128	127- 64	63 - 32	31 - 16
INIT_02	767 - 512	383 - 256	191 - 128	95 - 64	47 - 32
INIT_03	1023 - 768	511 - 384	255 - 192	127 - 96	63 - 48
INIT_04	1279 - 1024	639 - 512	319 - 256	159 - 128	79 - 64
INIT_05	1535 - 1280	767 - 640	383 - 320	191 - 160	95 - 80
INIT_06	1791 - 1536	895 - 768	447 - 384	223 - 192	111 - 96
INIT_07	2047 - 1792	1023 - 896	511 - 448	255 - 224	127 - 112
INIT_08	2303 - 2048	1151 - 1024	575 - 512	287 - 256	143 - 128
INIT_09	2559 - 2304	1279 - 1152	639 - 576	319 - 288	159 - 144
INIT_0A	2815 - 2560	1407 - 1280	703 - 640	351 - 320	175 - 160
INIT_0B	3071 - 2816	1535 - 1408	767 - 704	383 - 352	191 - 176
INIT_0C	3327 - 3072	1663 - 1536	831 - 768	415 - 384	207 - 192
INIT_0D	3583 - 3328	1791 - 1664	895 - 832	447 - 416	223 - 208
INIT_0E	3839 - 3584	1919 - 1792	959 - 896	479 - 448	239 - 224
INIT_0F	4095 - 3840	2047 - 1920	1023 - 960	511 - 480	255 - 240

Table 61-2: **RAMB16 INIT_xx Data Memory Addresses**

INIT_*xx*	RAMB16 Data Memory Addresses					
	16384 x 1	**8192 x 2**	**4096 x 4**	**2048 x 8**	**1024 x 16**	**512 x 32**
INIT_00	255 - 0	127 - 0	63 - 0	31 - 0	15 - 0	7 - 0
INIT_01	511- 256	255 - 128	127- 64	63 - 32	31 - 16	15 - 8
INIT_02	767- 512	383 - 256	191 - 128	95 - 64	47 - 32	23 - 16
INIT_03	1023 - 768	511 - 384	255 - 192	127 - 96	63 - 48	31 - 24
INIT_04	1279 - 1024	639 - 512	319 - 256	159 - 128	79 - 64	39 - 32
INIT_05	1535 - 1280	767 - 640	383 - 320	191 - 160	95 - 80	47 - 40
INIT_06	1791 - 1536	895 - 768	447 - 384	223 - 192	111 - 96	55 - 48
INIT_07	2047- 1792	1023 - 896	511 - 448	255 - 224	127 - 112	63 - 56
INIT_08	2303 - 2048	1151 - 1024	575 - 512	287 - 256	143 - 128	71 - 64
INIT_09	2559 - 2304	1279 - 1152	639 - 576	319 - 288	159 - 144	79 - 72
INIT_0A	2815 - 2560	1407 - 1280	703 - 640	351 - 320	175 - 160	87 - 80
INIT_0B	3071- 2816	1535 - 1408	767 - 704	383 - 352	191 - 176	95 - 88
INIT_0C	3327- 3072	1663 - 1536	831 - 768	415 - 384	207 - 192	103 - 96
INIT_0D	3583 - 3328	1791 - 1664	895 - 832	447 - 416	223 - 208	111 - 104
INIT_0E	3839 - 3584	1919 - 1792	959 - 896	479 - 448	239 - 224	119 - 112
INIT_0F	4095 - 3840	2047 - 1920	1023 - 960	511 - 480	255 - 240	127 - 120
INIT_10	4351 - 4096	2175- 2048	1087- 1024	543-512	271 - 256	135 - 128
INIT_11	4607- 4352	2303 -2176	1151 - 1088	575-544	287 - 272	143 - 136
INIT_12	4863- 4608	2431 - 2304	1215 - 1152	607- 576	303 - 288	151 - 144
INIT_13	5119- 4864	2559-2432	1279- 1216	639 -608	319 - 304	159 - 152
INIT_14	5375 - 5120	2687 - 2560	1343 -1280	671 - 640	335 - 320	167 - 160
INIT_15	5631 - 5376	2815-2688	1407- 1344	703 - 672	351 - 336	175 - 168
INIT_16	5887- 5632	2943 -2816	1471- 1408	735-704	367 - 352	183 - 176
INIT_17	6143- 5888	3071 -2944	1535- 1472	765-736	383 - 368	191 - 184
INIT_18	6399 - 6144	3199- 3072	1599 -1536	799-768	399 - 384	199 - 192
INIT_19	6655- 6400	3327 - 3200	1663 - 1600	831-800	415 - 400	207 - 200
INIT_1A	6911- 6656	3455 -3328	1727- 1664	863 - 832	431 - 416	215 - 208
INIT_1B	7167- 6912	3583 - 3456	1791- 1728	895- 864	447 - 432	223 - 216

Table 61-2: **RAMB16 INIT_xx Data Memory Addresses**

INIT_*xx*	RAMB16 Data Memory Addresses					
	16384 x 1	**8192 x 2**	**4096 x 4**	**2048 x 8**	**1024 x 16**	**512 x 32**
INIT_1C	7423 - 7168	3711 -3584	1855 - 1792	927-896	463 - 448	231 - 224
INIT_1D	7679 - 7424	3839 -3712	1919 - 1856	959 - 928	479 - 464	239 - 232
INIT_1E	7935 - 7680	3967 - 3840	1984 - 1920	991 -960	497 -480	247 - 240
INIT_1F	8191 - 7936	4095 -3968	2047-1984	1023 -992	511 - 496	255 - 248
INIT_20	8447 - 8192	4223 -4096	2111-2048	1055- 1024	527 - 512	263 - 256
INIT_21	8703 - 8448	4351 -4224	2175- 2112	1087- 1056	543 - 528	271 - 264
INIT_22	8959 - 8704	4479 -4352	2249 - 2176	1119 -1088	559 - 544	279 - 272
INIT_23	9215 - 8960	4507 -4480	2303- 2240	1151 -1120	575 - 560	287 - 280
INIT_24	9471 - 9216	4735-4608	2367 -2304	1183 -1152	591 - 576	295 - 288
INIT_25	9727 - 9472	4863-4736	2431- 2368	1215-1184	607 - 592	303 - 296
INIT_26	9983 - 9728	4991 -4864	2495 - 2432	1247 -1216	623 - 608	311 - 304
INIT_27	10239 - 9984	5119-4992	2559 - 2496	1279- 1248	639 - 624	319 - 312
INIT_28	10495 -10240	5247 - 5120	2623- 2560	1311 - 1280	655 - 640	327 - 320
INIT_29	10751 -10496	5375 - 5248	2687-2624	1343 - 1312	671 - 656	335 - 328
INIT_2A	11007 -10752	5503 - 5376	2751- 2688	1375 - 1344	687 - 672	343 - 336
INIT_2B	11263 - 11008	5631 -5504	2815- 2752	1407 -1376	703 - 688	351 - 344
INIT_2C	11519 - 11264	5759 -5632	2879-2816	1439 -1408	719 - 704	359 - 352
INIT_2D	11775 - 11520	5887-5760	2943- 2880	1471 - 1440	735 - 720	367 - 360
INIT_2E	12031 -11776	6015 -5888	3007- 2944	1503 -1472	751 - 736	375 - 368
INIT_2F	12287-12032	6143 - 6016	3071 - 3008	1535 - 1504	767 - 752	383 - 376
INIT_30	12543-12288	6271 -6144	3135- 3072	1567- 1536	783 - 768	391 - 384
INIT_31	12799-12544	6399 -6272	3199- 3136	1599-1568	799 - 784	399 - 392
INIT_32	13055-12800	6527- 6400	3263 -3200	1631 - 1600	815 - 800	407 - 400
INIT_33	13311-13056	6655 - 6528	3327- 3264	1663 -1632	831 - 816	415 - 408
INIT_34	13567-13312	6783-6656	3391-3328	1695 - 1664	847 - 832	423 - 416
INIT_35	13823-13568	6911-6784	3455 - 3392	1727-1696	863 - 848	431 - 424
INIT_36	14079 -13824	7039 - 6912	3519-3456	1759 -1728	879 - 864	439 - 432
INIT_37	14335-14080	7167 -7040	3583- 3520	1791 - 1760	895 - 880	447 - 440
INIT_38	14591-14336	7295 -7168	3647 - 3584	1823 - 1792	911 - 896	455 - 448

Table 61-2: **RAMB16 INIT_xx Data Memory Addresses**

INIT_*xx*	RAMB16 Data Memory Addresses					
	16384 x 1	**8192 x 2**	**4096 x 4**	**2048 x 8**	**1024 x 16**	**512 x 32**
INIT_39	14847-14592	7423 - 7296	3711 - 3648	1855 - 1824	927 - 912	463 - 456
INIT_3A	15103-14848	7551 -7424	3775- 3712	1887 - 1856	943 - 928	471 - 464
INIT_3B	15359-15104	7679- 7552	3839- 3776	1919 - 1888	959 - 944	479 - 472
INIT_3C	15615 -15360	7807 -7680	3903 - 3840	1951 - 1920	975 - 960	487 - 480
INIT_3D	15871-15616	7935 -7808	3967 - 3904	1983 -1952	993 - 976	495 - 488
INIT_3E	16128-15872	8063 -7936	4031 - 3968	2015 - 1984	1007 - 992	503 - 496
INIT_3F	16383-16128	8191 -8064	4095 - 4032	2047 - 2016	1023 - 1008	511 - 504

INIT_xx usage rules

A summary of the rules for INIT_*xx* follows.

- If INIT_*xx* is not attached to a block RAM, the contents of the RAM defaults to zero.
- Each initialization string defines 256 bits of the 4096-bit or 16384-bit data memory of the block RAM. For example, for a 4096-bit deep x 1-bit wide block RAM, INIT_00 assigns the 256 bits to addresses 0 through 255 and INIT_01 assigns the 256 bits to addresses 256 through 511. For a 2048-bit deep x 2-bit wide block RAMs, INIT_00 assigns the 256 bits to addresses 0 through 127 (a 2-bit value at each address) and INIT_01 assigns the 256 bits to addresses 128 through 255.
- If a subset of the INIT_00 through INIT_0F properties is specified for a 4096-bit RAMB4 or a subset of the INIT_00 through INIT_3F properties for the 16384-bit data memory of a RAMB16, the remaining properties default to zero.
- In an initialization string, the least significant bit (LSB) is the right-most value.
- The least significant word of the block RAM address space specified by INIT_*xx* is composed of the least significant bits of the block RAM INIT_*xx* constraint.

INIT_xx on block RAMs of various widths

The initialization string "fills" the block RAM beginning from the LSB of the 256 bits for the specified INIT_xx addresses. The size of the word filling each address depends on the width of the block RAM being initialized— 1, 2, 4, 8, 16, or 32 bits.

For example for a RAMB4, if INIT_0C=bcde7, the corresponding binary sequence is as follows:

1011	1100	1101	1110	0111	←LSB
b	c	d	e	7	

The appropriate addresses in the RAM are initialized with the binary string content depending on the width of the RAM as shown in the following table.

Block RAM (depth x width)	Address (INIT_0C)	Contents
4096 x 1	3072 3073 3074 3075 . 3327	1 1 1 0 . 0
2048 x 2	1536 1537 1538 1539 . 1663	11 01 10 11 . 00
1024 x 4	768 769 770 771 . 831	0111 1110 1101 1100 . 0000
512 x 8	384 385 386 387 . 415	11100111 11001101 00001011 00000000 . 00000000
256 x 16	192 193 194 195 . 207	1100110111101111 0000000000001011 0000000000000000 0000000000000000 . 0000000000000000

XCF

```
BEGIN MODEL "entity_name"
 INST "instance_name" init_xx=value;
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

INITP_xx

INITP_*xx* Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

INITP_*xx* Applicable Elements

- RAMB16_S9
- RAMB16_S18
- RAMB16_S36
- RAMB16_S1_S9, 18, 36
- RAMB16_S2_S9, 18, 36
- RAMB16_S4_S9, 18, 36
- RAMB16_S9_S9, 18, 36
- RAMB16_S18_S18, 36
- RAMB16_S36_S36

INITP_*xx* Description

INITP_*xx* is a basic initialization constraint. INITP_00 through INITP_07 specifies the initialization strings for the parity memory of RAMB16 components.

INITP_*xx* Propagation Rules

It is illegal to attach INITP_*xx* to a net or signal. When attached to a design element, INITP_*xx* propagates to all applicable elements in the hierarchy within the design element.

INITP_*xx* Syntax Examples

Schematic

Attach to a logic symbol.

Attribute Name—INITP_*xx*

Attribute Values—*value*

See the UCF section for a description of *value*.

VHDL

Before using INITP_xx, declare it with the following syntax:

```
attribute initp_xx: string;
```

After INITP_xx has been declared, specify the VHDL constraint as follows:

```
attribute initp_xx of {component_name|label_name}: {component|label} is
"value";
```

For a discussion of *value*, see the UCF section.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute initp_xx [of] {module_name|instance_name} [is]
value;
```

For a discussion of *value*, see the UCF section.

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

The basic syntax is:

```
INST "instance_name" INITP_xx=value;
```

where

- *xx* is a two-digit hexadecimal value 00 through 07 that specifies which 256 bits (see the following table) of the 2048-bit block RAM parity data to initialize to the specified value.
- *value* is a string of hexadecimal characters up to 64 digits wide. If the INIT_xx constraint has a value less than the required 64 hex digits, the value will be padded with zeros from the most significant bit (MSB) side. This fills the 256 bits in the initialization string (4 bits per hexadecimal character * 64 characters0.

Table 62-1: **RAMB16 Addresses for INITP_*xx***

INITP_*xx*	**RAMB16 Addresses**		
	2048 x 1	**1024 x 2**	**512 x 4**
INITP_00	255 - 0	127 - 0	63 - 0
INITP_01	511 - 256	255 - 128	127- 64
INITP_02	767 - 512	383 - 256	191 - 128
INITP_03	1023 - 768	511 - 384	255 - 192
INITP_04	1279 - 1024	639 - 512	319 - 256
INITP_05	1535 - 1280	767 - 640	383 - 320
INITP_06	1791 - 1536	895 - 768	447 - 384
INITP_07	2047 - 1792	1023 - 896	511 - 448

The following statement specifies that the INITP_03 addresses in instance foo/bar be initialized, starting from the LSB, to the hex value aaaaaaaaaaaaaaaaaaaa (padded with 44 zeros from the MSB side).

```
INST “foo/bar” INITP_03=aaaaaaaaaaaaaaaaaaaa;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

INREG

INREG Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	No
Spartan-3E	No
Virtex-II	No
Virtex-II Pro	No
Virtex-II Pro X	No
Virtex-4	No
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

INREG Applicable Elements

Applies to register and latch instances with their D-inputs driven by input pads or to the Q-output nets of such registers or latches.

INREG Description

This constraint applies to register and latch instances with their D-inputs driven by input pads, or to the Q-output nets of such registers and latches. By default, registers and latches in a CoolRunner XPLA3 or CoolRunner-II design that have their D-inputs driven by input pads are automatically implemented using the device's Fast Input path, where possible. If you disable the Project Navigator property Use Fast Input for Input Registers for the Fit (Implement Design) process, then only register and latches with the INREG attribute are considered for Fast Input optimization.

INREG Propagation Rules

Applies to register or latch to which it is attached or to the Q-output nets of such registers or latches.

INREG Syntax Examples

Schematic

Attach to a register, latch, or net.

Attribute Name—INREG

Attribute Values—None (TRUE by default)

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

```
XILINX PROPERTY 'inreg signal_name';
```

UCF

```
NET “signal_name” INREG;
INST “register_name” INREG;
```

NCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

XCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

IOB

IOB Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

IOB Applicable Elements

Non-INFF/OUTFF flip-flop and latch primitives, registers

IOB Description

IOB is a basic mapping and synthesis constraint. It indicates which flip-flops and latches can be moved into the IOB. The mapper supports a command line option (-pr i | o | b) that allows flip-flop or latch primitives to be pushed into the input IOB (i), output IOB (o), or input/output IOB (b) on a global scale. The IOB constraint, when associated with a flip-flop or latch, tells the mapper to pack that instance into an IOB type component if possible. The IOB constraint has precedence over the mapper **-pr** command line option.

XST considers the IOB constraint as an implementation constraint, and will therefore propagate it in the generated NGC file.

XST also duplicates the flip-flops and latches driving the Enable pin of output buffers, so that the corresponding flip-flops and latches can be packed in the IOB.

IOB Propagation Rules

Applies to the design element to which it is attached.

IOB Syntax Examples

Schematic

Attach to a flip-flop or latch instance or to a register.

Attribute Name—IOB

Attribute Values—TRUE, FALSE, AUTO

VHDL

Before using IOB, declare it with the following syntax:

```
attribute iob: string;
```

After IOB has been declared, specify the VHDL constraint as follows:

```
attribute iob of {component_name|entity_name|label_name}:
{component|entity|label} is "(true|false|auto)";
```

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute iob [of] {module_name|instance_name} [is]
(true|false|auto);
```

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

The basic syntax is:

```
INST "instance_name" IOB={TRUE|FALSE|AUTO};
```

where

- **TRUE** allows the flip-flop or latch to be pulled into an IOB
- **FALSE** indicates not to pull it into an IOB
- **AUTO**, XST takes into account timing constraints and will automatically decide to push or not to push flip-flops into IOBs.

The following statement instructs the mapper from placing the foo/bar instance into an IOB component.

```
INST "foo/bar" IOB=TRUE;
```

XCF

```
BEGIN MODEL "entity_name"
```

```
 NET “signal_name” iob={true|false|auto};
 INST “instance_name” iob={true|false|auto};
END;
```

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

In the Misc tab, click Specify next to “Registers to be placed in IOBs“ and move the desired register to the Registers for IOB packing list. This sets the IOB constraint to TRUE.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-iob** command line option of the **run** command. Following is the basic syntax:

```
-iob {true|false|auto}
```

The default is Auto.

Project Navigator

You can specify IOB globally with the Pack I/O Registers into IOBs option in the Xilinx Specific Options tab of the Process Properties dialog box within the Project Navigator. YES maps to TRUE. NO maps to FALSE.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

IOBDELAY

IOBDELAY Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

IOBDELAY Applicable Elements

Any I/O symbol (I/O pads, I/O buffers, or input pad nets)

IOBDELAY Description

IOBDELAY is a basic mapping constraint. It specifies how the input path delay elements in Spartan-II, Spartan-IIE, Spartan-3, Virtex, Virtex-E, Virtex-II, Virtex-II Pro, and Virtex-II Pro X devices are to be programmed. There are two possible destinations for input signals: the local IOB input FF or a load external to the IOB. Spartan-II, Spartan-3, Virtex, Virtex-E, Virtex-II, Virtex-II Pro, and Virtex-II Pro X devices allow a delay element to delay the signal going to one or both of these destinations.

IOBDELAY cannot be used concurrently with NODELAY.

IOBDELAY Propagation Rules

Although IOBDELAY is attached to an I/O symbol, it applies to the entire I/O component.

IOBDELAY Syntax Examples

Schematic

Attach to an I/O symbol.

Attribute Name—IOBDELAY

Attribute Values—NONE, BOTH, BUF, IFD

VHDL

Before using IOBDELAY, declare it with the following syntax:

```
attribute iobdelay: string;
```

After IOBDELAY has been declared, specify the VHDL constraint as follows:

```
attribute iobdelay of {component_name|label_name}: {component|label} is
"{NONE|BOTH|IBUF|IFD}";
```

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute iobdelay [of] {module_name|instance_name} [is]
{NONE|BOTH|IBUF|IFD};
```

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name" IOBDELAY={NONE|BOTH|IBUF|IFD};
```

where

- NONE, the default, sets the delay OFF for both the IBUF and IFD paths.
- BOTH sets the delay ON for both the IBUF and IFD paths.
- IBUF sets the delay to OFF for any register inside the I/O component and to ON for the register(s) outside of the component if the input buffer drives a register D pin outside of the I/O component.
- IFD sets the delay to ON for any register inside the I/O component and to OFF for the register(s) outside the component if a register occupies the input side of the I/O component, regardless of whether the register has the IOB=TRUE constraint.

The following statement sets the delay OFF for the IBUF and IFD paths.

```
INST "xyzzy" IOBDELAY=NONE;
```

XCF

Not applicable.

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

In the Ports tab grid with the I/O Configuration Options checked, click the IOBDELAY column in the row with the desired input port name and choose a value from the drop down list.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

IOSTANDARD

IOSTANDARD Architecture Support

Note: The numbers in the second column are explained in the next section, "IOSTANDARD Applicable Elements".

Architecture	Supported/Unsupported
Virtex	1
Virtex-E	1, 2, 3
Spartan-II	1
Spartan-IIE	1, 2, 3
Spartan-3	1, 2
Spartan-3E	1, 2
Virtex-II	1, 2
Virtex-II Pro	1, 2
Virtex-II Pro X	1, 2
Virtex-4	1, 2
XC9500, XC9500XL, XC9500XV	3
CoolRunner XPLA3	No
CoolRunner-II	1, 3

IOSTANDARD Applicable Elements

1. IBUF, IBUFG, OBUF, OBUFT
2. IBUFDS, IBUFGDS, OBUFDS, OBUFTDS
3. Output Voltage Banks

IOSTANDARD Description

IOSTANDARD is a basic mapping constraint and synthesis constraint.

IOSTANDARD for FPGAs

Use IOSTANDARD to assign an I/O standard to an I/O primitive.

All components with IOSTANDARD must follow the same placement rules (banking rules) as the SelectIO components. See the Libraries Guide for information on the banking rules for each architecture and for descriptions of the supported I/O standards.

For Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X, the recommended procedure is to attach IOSTANDARD to a buffer component instead of using the SelectIO variants of a component. For example, use an IBUF with the IOSTANDARD=HSTL_III constraint instead of the IBUF_HSTL_III component.

For Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X, differential signaling standards apply to IBUFDS, IBUFGDS, OBUFDS, and OBUFTDS only (not IBUF or OBUF).

IOSTANDARD for CPLDs

You can apply IOSTANDARD to I/O pads of CoolRunner-II devices to specify both input threshold and output VCCIO voltage. See the table under the UCF section for supported values.

You can apply IOSTANDARD to outputs of XC9500XV devices to specify the VCCO voltage. The IOSTANDARD names supported by XC9500XV are:

- LVTTL (VCCO=3.3V)
- LVCMOS2 (VCCO=2.5V)
- X25TO18 (VCCO=1.8V).

The X25TO18 setting is provided for generating 1.8V compatible outputs from a CPLD normally operating in a 2.5V environment.

The CPLD fitter automatically groups outputs with compatible IOSTANDARD settings into the same bank when no location constraints are specified.

IOSTANDARD Propagation Rules

It is illegal to attach IOSTANDARD to a net or signal except when the signal or net is connected to a pad. In this case, IOSTANDARD is treated as attached to an IOB instance (IBUF, OBUF, IOB FF). When attached to a design element, IOSTANDARD propagates to all applicable elements in the hierarchy within the design element.

IOSTANDARD Syntax Examples

Schematic

Attach to an I/O primitive.

Attribute Name—IOSTANDARD

Attribute Values—*iostandard_name*

See the UCF section.

VHDL

Before using IOSTANDARD, declare it with the following syntax:

```
attribute iostandard: string;
```

After IOSTANDARD has been declared, specify the VHDL constraint as follows:

```
attribute iostandard of {component_name|label_name}: {component|label}
is "iostandard_name";
```

See the UCF section for a description of *iostandard_name*.

For CPLDs you can also apply IOSTANDARD to the pad signal.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
// synthesis attribute iostandard [of] {module_name|instance_name}
[is] iostandard_name;
```

See the UCF section for a description of *iostandard_name*.

For CPLDs you can also apply IOSTANDARD to the pad signal.

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

```
XILINX PROPERTY 'iostandard=iostandard_name mysignal';
```

UCF/NCF

The basic syntax is:

```
INST "instance_name" IOSTANDARD=iostandard_name;
NET "pad_net_name" IOSTANDARD=iostandard_name;
```

where *iostandard_name* is an IO Standard name as specified in the following sections.

For IBUF, IBUFG, OBUF, or OBUFT SelectIO Buffers

The default is LVTTL (except Virtex-II Pro and Virtex-II Pro X) if no IOSTANDARD constraint is specified. The default for Virtex-II Pro and Virtex-II Pro X is LVCMOS25.

The variable *iostandard_name* can have the following values depending on the targeted architecture.

Table 66-1: **IBUF, IBUFG, OBUF, or OBUFT SelectIO Buffers**

iostandard name	Spartan-II, Virtex	Virtex-E, Spartan-IIE	Spartan-3	Virtex-II	Virtex-II Pro and Virtex-II Pro X	9500XV	Cool Runner-II
AGP	√	√		√			
GTL	√	√	√	√	√		
GTL_DCI			√	√	√		
GTLP	√	√	√	√	√		
GTLP_DCI			√	√	√		
HSTL_I	√	√	√	√	√		√**
HSTL_I_18[A]			√	√	√		
HSTL_I_DCI			√	√	√		
HSTL_I_DCI_18			√	√	√		

Table 66-1: **IBUF, IBUFG, OBUF, or OBUFT SelectIO Buffers**

iostandard name	Spartan-II, Virtex	Virtex-E, Spartan-IIE	Spartan-3	Virtex-II	Virtex-II Pro and Virtex-II Pro X	9500XV	Cool Runner-II
HSTL_II			√	√	√		
HSTL_II_18			√	√	√		
HSTL_II_DCI			√	√	√		
HSTL_II_DCI_18			√	√	√		
HSTL_III	√	√	√	√	√		
HSTL_III_18			√	√	√		
HSTL_III_DCI			√	√	√		
HSTL_III_DCI_18			√	√	√		
HSTL_IV	√	√		√	√		
HSTL_IV_18				√	√		
HSTL_IV_DCI				√	√		
HSTL_IV_DCI_18				√	√		
LDT_25_DT					√		
LVCMOS2	√	√				√	
LVCMOS12			√				
LVCMOS15			√	√	√		√*
LVCMOS18		√	√	√	√		√
LVCMOS25			√	√	√		√
LVCMOS33			√	√	√		√
LVDCI_15			√	√	√		
LVDCI_18			√	√	√		
LVDCI_25			√	√	√		
LVDCI_33			√	√	√		
LVDCI_DV2_15			√	√	√		
LVDCI_DV2_18			√	√	√		
LVDCI_DV2_25			√	√	√		
LVDCI_DV2_33			√	√			
LVDS		√					
LVDS_25_DT					√		
LVDSEXT_25_DT					√		
LVTTL (default)	√	√	√	√	√	√	√
PCI33_3	√	√	√	√	√		
PCI33_5	√						
PCI66_3	√	√		√	√		
PCIX				√	√		
PCIX66_3		√					

Table 66-1: **IBUF, IBUFG, OBUF, or OBUFT SelectIO Buffers**

iostandard name	Spartan-II, Virtex	Virtex-E, Spartan-IIE	Spartan-3	Virtex-II	Virtex-II Pro and Virtex-II Pro X	9500XV	Cool Runner-II
SSTL18_I			√	√	√		
SSTL18_I_DCI			√	√	√		
SSTL18_II				√	√		
SSTL18_II_DCI			√	√	√		
SSTL2_I	√	√	√	√	√		√**
SSTL2_I_DCI			√	√	√		
SSTL2_II	√	√	√	√	√		
SSTL2_II_DCI			√	√	√		
SSTL3_I	√	√		√			√**
SSTL3_I_DCI				√			
SSTL3_II	√	√		√			
SSTL3_II_DCI				√			
ULVDS_25_DT					√		
X25TO18						√	

* For CoolRunner-II, LVCMOS15 automatically configures the input structure with Schmitt Trigger.

** Supported for CoolRunner-II devices with 128 macrocells and larger.

A - This IOSTANDARD is available in both PACE and the Constraints Editor.

Differential Signaling

BLVDS_* and LVPECL_* are the only available bidirectional standards for differential signaling. Other IOSTANDARD values can be bidirectional, as long as they are not for differential signaling. So, for instance, LVTTL can always be bidirectional.

- For IBUFDS, IBUFDS_DIFF_OUT, IBUFGDS, and IBUFGDS_DIFF_OUT

  The variable *iostandard_name* can have the following values:

  - BLVDS_25 (Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X)
    (BLVDS is not supported for IBUFDS_DIFF_OUT and IBUFGDS_DIFF_OUT)
  - LDT_25 (Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X)
  - LVDS (Virtex-E, Spartan-IIE)
  - LVDS_25 (Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X)
    This is the default for Virtex-II Pro and Virtex-II Pro X.
  - LVDS_25_DCI (Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X)
  - LVDS_33 is the default for Virtex-II.
  - LVDSEXT_25 (Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X)
  - LVDSEXT_25_DCI (Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X)
  - LVDSEXT_33 (Virtex-II)
  - LVPECL_25 (Virtex-II Pro, and Virtex-II Pro X)
  - LVPECL_33 (Virtex-II)
  - ULVDS_25 (Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X

- For IOBUFDS

  BLVDS_25 (Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X)

- For OBUFDS or OBUFTDS

  The default is LVDS_33 if no IOSTANDARD constraint is specified.

  The variable *iostandard_name* can have the following values:

  - BLVDS_25 (Virtex-II, Virtex-II Pro, and Virtex-II Pro X)
  - LDT_25 (Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X)
  - LVDS_25 (Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X)
    This is the default for Virtex-II Pro and Virtex-II Pro X.
  - LVDS_33 (Virtex-II)
    This is the default for Virtex-II.
  - LVDSEXT_25 (Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X)
  - LVDSEXT_33 (Virtex-II)
  - LVPECL_25 (Virtex-II Pro, and Virtex-II Pro X)
  - LVPECL_33 (Virtex-II)
  - ULVDS_25 (Virtex-II, Virtex-II Pro, and Virtex-II Pro X)

For XC9500XV Output Voltage Banks

The default is LVTTL if no IOSTANDARD constraint is specified.

The variable *iostandard_name* can have the following values:

- LVCMOS2
- LVTTL (default)
- X25TO18 (for voltage translation from 2.5V to 1.8V)

XCF

```
BEGIN MODEL "entity_name"
 INST "instance_name" iostandard=string;
 NET "signal_name" iostandard=string;
END;
```

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

In the Ports tab grid with the I/O Configuration Options checked, click the IOSTANDARD column in the row with the desired net name and choose a value from the drop down list.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

The Pin Assignments Editor is mainly used for assigning location constraints to IOs in designs but can also be used to assign certain IO properties like IO Standards. You can access PACE from the Processes window in the Project Navigator. Double-click Assign Package Pins or Create Area Constraints under User Constraints. In the Design Object List -- I/O Pins window, select a value from the I/O Std column.

For details on how to use PACE, see the PACE online help, especially the topics within Editing Pins and Areas in the Procedures section.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

KEEP

KEEP Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

KEEP Applicable Elements

Signals

KEEP Description

KEEP is an advanced mapping constraint and synthesis constraint. When a design is mapped, some nets may be absorbed into logic blocks. When a net is absorbed into a block, it can no longer be seen in the physical design database. This may happen, for example, if the components connected to each side of a net are mapped into the same logic block. The net may then be absorbed into the block containing the components. KEEP prevents this from happening.

KEEP is translated into an internal constraint known as NOMERGE when targeting an FPGA. Messaging from the implementation tools will therefore refer to the system property NOMERGE—not KEEP.

KEEP Propagation Rules

Applies to the signal to which it is attached.

KEEP Syntax Examples

Schematic

Attach to a net.

Attribute Name—KEEP

Attribute Values—TRUE, FALSE

VHDL

Before using KEEP, declare it with the following syntax:

```
attribute keep : string;
```

After KEEP has been declared, specify the VHDL constraint as follows:

```
attribute keep of signal_name: signal is “true”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute keep [of] signal_name [is] “true”;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

```
mysignal NODE istype ‘keep’;
```

UCF/NCF

The following statement ensures that the net $SIG_0 will remain visible.

```
NET “$1I3245/$SIG_0” KEEP;
```

XCF

```
BEGIN MODEL “entity_name”
 NET “signal_name” keep={yes|no|true|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

KEEP_HIERARCHY

KEEP_HIERARCHY Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

KEEP_HIERARCHY Applicable Elements

KEEP_HIERARCHY is attached to logical blocks, including blocks of hierarchy or symbols.

KEEP_HIERARCHY Description

KEEP_HIERARCHY is a synthesis and implementation constraint. If hierarchy is maintained during Synthesis, the Implementation tools will use this constraint to preserve the hierarchy throughout the implementation process and allow a simulation netlist to be created with the desired hierarchy.

XST may flatten the design to get better results by optimizing entity or module boundaries. You can set KEEP_HIERARCHY to **`true`** so that the generated netlist is hierarchical and respects the hierarchy and interface of any entity or module of your design.

This option is related to the hierarchical blocks (VHDL entities, Verilog modules) specified in the HDL design and does not concern the macros inferred by the HDL synthesizer. Three values are available for this option:

- **`true`**: allows the preservation of the design hierarchy, as described in the HDL project. If this value is applied to synthesis, it will also be propagated to implementation.
- **`false`**: hierarchical blocks are merged in the top level module.
- **`soft`**: allows the preservation of the design hierarchy in synthesis, but the KEEP_HIERARCHY constraint is not propagated to implementation.

For CPLDs, the default is **`true`**. For FPGAs, the default is **`false`**.

In general, an HDL design is a collection of hierarchical blocks, and preserving the hierarchy gives the advantage of fast processing because the optimization is done on separate pieces of reduced complexity. Nevertheless, very often, merging the hierarchy blocks improves the fitting results (fewer PTerms and device macrocells, better frequency) because the optimization processes (collapsing, factorization) are applied globally on the entire logic.

The keep_hierarchy constraint enables or disables hierarchical flattening of user-defined design units. Allowed values are **`true`** and **`false`**. By default, the user hierarchy is preserved.

In the following figure, if KEEP_HIERARCHY is set to the entity or module I2, the hierarchy of I2 will be in the final netlist, but its contents I4, I5 will be flattened inside I2. Also I1, I3, I6, I7 will be flattened.

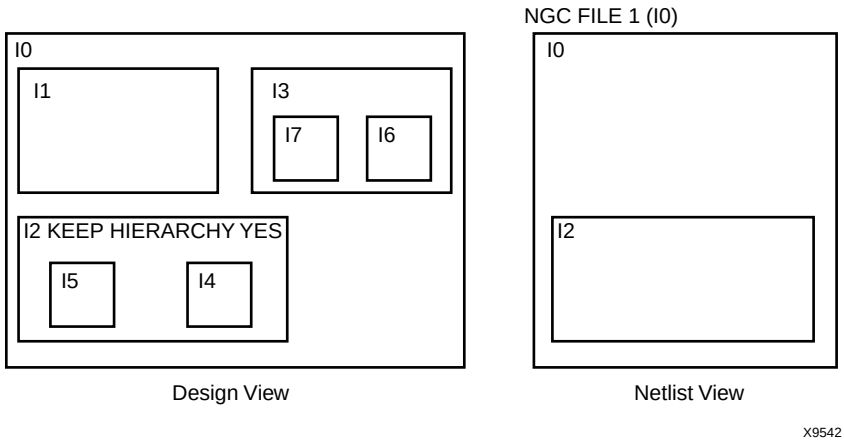


Figure 68-1: **KEEP_HIERARCHY EXAMPLE**

KEEP_HIERARCHY Propagation Rules

Applies to the entity or module to which it is attached.

KEEP_HIERARCHY Syntax Examples

Schematic

Attach to the entity or module symbol.

Attribute Name—KEEP_HIERARCHY

Attribute Values—TRUE, FALSE

VHDL

Before using KEEP_HIERARCHY, declare it with the following syntax:

```
attribute keep_hierarchy : string;
```

After KEEP_HIERARCHY has been declared, specify the VHDL constraint as follows:

```
attribute keep_hierarchy of architecture_name: architecture is
true|false|soft;
```

The default is **false** for FPGAs and **true** for CPLDs.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute keep_hierarchy [of] module_name [is]
{true|false|soft};
```

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

For instances:

```
INST "instance_name" KEEP_HIERARCHY={true|false|soft};
```

XCF

```
MODEL "entity_name" keep_hierarchy={true|false|soft};
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-keep_hierarchy** command line option of the **run** command. Following is the basic syntax:

```
-keep_hierarchy {true|false|soft}
```

The default is **false** for FPGAs and **true** for CPLDs.

See Chapter 8, “Command Line Mode,” in the *XST User Guide* for details.

Project Navigator

Set KEEP_HIERARCHY globally with the Keep Hierarchy option in the Synthesis Options tab of the Process Properties dialog box within the Project Navigator. With a design selected in the Sources window, right-click Synthesize in the Processes window to access the Process Properties dialog box.

KEEPER

KEEPER Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	Yes

KEEPER Applicable Elements

Tri-state input / output pad nets.

KEEPER Description

KEEPER is a basic mapping constraint. It retains the value of the output net it is attached to. For example, if logic 1 is being driven onto the net, KEEPER drives a weak / resistive 1 onto the net. If the net driver is then 3-stated, KEEPER continues to drive a weak / resistive 1 onto the net.

The KEEPER constraint must follow the same banking rules as the KEEPER component. See the *Libraries Guide* for information on the banking rules.

KEEPER, PULLUP, and PULLDOWN are only valid on pad NETs, not on INSTs of any kind.

Note: For CoolRunner-II designs, the use of KEEPER and the use of PULLUP are mutually exclusive across the whole device.

KEEPER Propagation Rules

KEEPER is illegal when attached to a net or signal except when the net or signal is connected to a pad. In this case, KEEPER is treated as attached to the pad instance.

KEEPER Syntax Examples

Schematic

Attach to an output pad net.

Attribute Name—KEEPER

Attribute Values—TRUE, FALSE

VHDL

Before using KEEPER, declare it with the following syntax:

```
attribute keeper: string;
```

After KEEPER has been declared, specify the VHDL constraint as follows:

```
attribute keeper of signal_name : signal is “yes”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

```
// synthesis attribute keeper [of] signal_name [is] “yes”;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

```
XILINX PROPERTY 'KEEPER mysignal';
```

UCF/NCF

These statement configures the IO to use KEEPER:

```
NET "pad_net_name" KEEPER;
```

XCF

```
BEGIN MODEL “entity_name”
 NET “signal_name” keeper={true|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

LOC

LOC Architecture Support

Note: The numbers indicate the applicable elements. See the LOC Applicable Elements section (following).

Architecture	Supported/Unsupported
Virtex	1, 2, 3, 5, 6, 7, 9, 10, 13
Virtex-E	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 13
Spartan-II	1, 2, 3, 5, 6, 7, 8, 9, 10, 13
Spartan-IIE	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 13
Spartan-3	1, 2, 3, 5, 7, 9, 10, 11, 12
Spartan-3E	1, 2, 3, 5, 7, 9, 10, 11, 12
Virtex-II	1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12
Virtex-II Pro	1, 2, 3, 5, 6, 7, 9, 10, 11, 12

Virtex-II Pro X	1, 2, 3, 5, 6, 7, 9, 10, 11, 12
Virtex-4	1, 2, 3, 5, 7, 9, 10, 11, 12
XC9500, XC9500XL, XC9500XV	1, 3, 9
CoolRunner XPLA3	1, 3, 9
CoolRunner-II	1, 3, 9

LOC Applicable Elements

1. Registers
2. FMAP
3. IO elements
4. ROM
5. RAMS, RAMD
6. BUFT
7. Clock buffers
8. Edge decoders
9. Any instance
10. Block RAMs
11. Multipliers
12. DCMs
13. DLLs

LOC Description

LOC is a basic placement constraint and a synthesis constraint.

LOC Description for FPGAs

LOC defines where a design element can be placed within an FPGA. It specifies the absolute placement of a design element on the FPGA die. It can be a single location, a range of locations, or a list of locations. You can specify LOC from the design file and also direct placement with statements in a constraints file.

To specify multiple locations for the same symbol, separate each location within the field using a comma. The comma specifies that the symbols can be placed in any of the specified locations. You can also specify an area in which to place a design element or group of design elements.

A convenient way to find legal site names is use the FPGA Editor, PACE, or Floorplanner. The legal names are a function of the target part type. To find the correct syntax for specifying a target location, load an empty part into the FPGA Editor (or look in the Floorplanner). Place the cursor on any block, then click the block to display its location in the FPGA Editor history area. Do not include the pin name such as .I, .O, or .T as part of the location.

You can use LOC for logic that uses multiple CLBs, IOBs, soft macros, or other symbols. To do this, use LOC on a soft macro symbol, which passes the location information down to the logic on the lower level. The location restrictions are automatically applied to all blocks on the lower level for which LOCs are legal.

Spartan-II, Spartan-IIE, Virtex, and Virtex-E

The physical site specified in the location value is defined by the row and column numbers for the array, with an optional extension to define the slice for a given row / column location. A Spartan-II, Spartan-IIE, Virtex, Virtex-E slice is composed of:

- two LUTs (which can be configured as RAM or shift registers)
- two flip-flops (which can also be configured as latches)
- two XORCYs
- two MULT_ANDs
- one MUXF5
- one MUXF6
- one MUXCY

Only one MUXF6 can be used between the two adjacent slices in a specific row / column location. The two slices at a specific row / column location are adjacent to one another.

The block RAMs (RAMB4s) have a different row / column grid specification than the CLB and TBUFs. A block RAM located at RAMB4_R3C1 is not located at the same site as a flip-flop located at CLB_R3C1. Therefore, the location value must start with "CLB," "TBUF," or "RAMB4." The location cannot be shortened to reference only the row, column, and extension. The optional extension specifies the left-most or right-most slice for the row / column.

The location value for global buffers and DLL elements is the specific physical site name for available locations.

Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X

In the Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X CLBs, there are four slices, arranged vertically, per CLB with the bottom two slices on the left side of the CLB and the top two slices on the right side of the CLB. Each slice is equivalent and contains two function generators (F and G), two storage elements, arithmetic logic gates, large multiplexers, wide function capability, and two fast carry look-ahead chains.

The Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X architectures diverge from the traditional Row / Column / Slice designators on the CLB. Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X use a Cartesian-based XY designator at the slice level. The slice-based location specification uses the form: SLICE_X*m*Y*n*. The XY slice grid starts as X0Y0 in the lower left CLB tile of the chip. The X values start at 0 and increase horizontally to the right in the CLB row, with two different X values per CLB. The Y values start at 0 and increase

vertically up in the CLB column, with two different Y values per CLB. The XY slice numbering scheme is shown in the following figure.

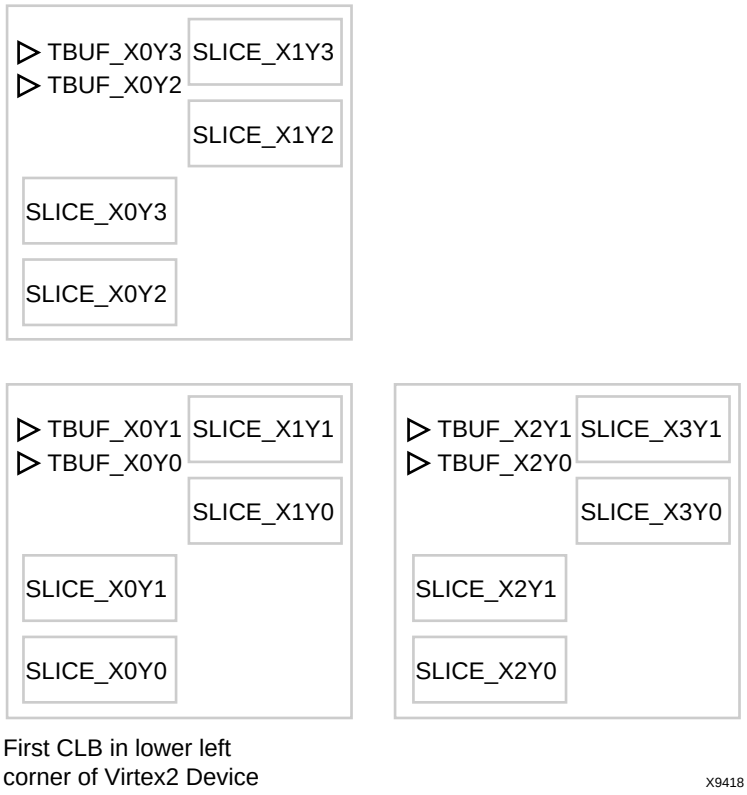


Figure 70-1: **Slice and TBUF Numbering in Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X**

Following are examples of how to specify the slices in the XY coordinate system.

SLICE_X0Y0	First (bottom) slice of the CLB in the lower left corner of the chip
SLICE_X0Y1	Second slice of the CLB in the lower left corner of the chip
SLICE_X1Y0	Third slice of the CLB in the lower left corner of the chip
SLICE_X1Y1	Fourth (top) slice of the CLB in the lower left corner of the chip
SLICE_X0Y2	First slice of the second CLB in CLB column 1
SLICE_X2Y0	First (bottom) slice of the bottom CLB in CLB column 2
SLICE_X2Y1	Second slice of the bottom CLB in CLB column 2
SLICE _X50Y125	Slice located 125 slices up from and 50 slices to the right of SLICE_X0Y0

The Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X block RAMs, TBUFs, and multipliers have their own specification different from the SLICE specifications. Therefore, the location value must start with "SLICE," "RAMB," "TBUF," or "MULT." The Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X block RAMs and multipliers have their own XY

grids different from the SLICE XY grid. A block RAM located at RAMB16_X2Y3 is not located at the same site as a flip-flop located at SLICE_X2Y3. A multiplier located at MULT18X18_X2Y3 is not located at the same site as a flip-flop located at SLICE_X2Y3 or at the same site as a block RAM located at RAMB16_X2Y3. However, the two TBUFs in each CLB follow the same XY grid as the SLICEs. A TBUF located at TBUF_X2Y3 is in the same CLB as a flip-flop located at SLICE_X2Y3.

Because there are two TBUFs per CLB and four slices per CLB, the X value for a TBUF is always an even integer or zero (for example, TBUF_X1Y1 is illegal).

The location values for global buffers and DLL elements is the specific physical site names for available locations.

LOC Description for CPLDs

For CPLDs, use the LOC=*pin_name* constraint on a PAD symbol or pad net to assign the signal to a specific pin. The PAD symbols are IPAD, OPAD, IOPAD, and UPAD. You can use the LOC=FBnn constraint on any instance or its output net to assign the logic or register to a specific function block or macrocell, provided the instance is not collapsed.

The LOC=FB*nn_mm* constraint on any internal instance or output pad assigns the corresponding logic to a specific function block or macrocell within the CPLD. If a LOC is placed on a symbol that does not get mapped to a macrocell or is otherwise removed through optimization, the LOC will be ignored.

Pin assignment using the LOC constraint is not supported for bus pad symbols such as OPAD8.

Location Specification Types for FPGAs

Use the following location types to define the physical location of an element

Table 70-1: **Location Types for FPGAs.**

Element Types	Location Examples	Meaning
IOBs:		
	P12	IOB location (chip carrier)
	A12	IOB location (pin grid)
	B, L, T, R	Applies to IOBs and indicates edge locations (bottom, left, top, right) for Spartan-II, Spartan-IIE, Spartan-3, Virtex, Virtex-E, Virtex-II, Virtex-II Pro, and Virtex-II Pro X.
	LB, RB, LT, RT, BR, TR, BL, TL	Applies to IOBs and indicates half edges (left bottom, right bottom, and so forth) for Spartan-II, Spartan-IIE, Spartan-3, Virtex, Virtex-E, Virtex-II, Virtex-II Pro, and Virtex-II Pro X.

Element Types	Location Examples	Meaning
	Bank0, Bank1, Bank2, Bank3, Bank4, Bank5, Bank6, Bank7	Applies to IOBs and indicates half edges (banks) for Spartan-II, Spartan-IIE, Spartan-3, Virtex, Virtex-E, Virtex-II, Virtex-II Pro, and Virtex-II Pro X.
CLBs:		
	CLB_R4C3 (or .S0 or .S1)	CLB location for Spartan-II, Spartan-IIE, Virtex, Virtex-E
	CLB_R6C8.S0 (or .S1)	Function generator or register slice for Spartan-II, Spartan-IIE, Virtex, Virtex-E
Slices:		
	SLICE_X22Y3	Slice location for Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X
TBUFs:		
	TBUF_R6C7 (or .0 or .1)	TBUF location for Spartan-II, Spartan-IIE, Virtex, Virtex-E
	TBUF_X6Y7	TBUF location for Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X
Block RAMs		
	RAMB4_R3C1	Block RAM location for Spartan-II, Spartan-IIE, Virtex, Virtex-E
	RAMB16_X2Y56	Block RAM location for Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X
Multipliers:		
	MULT18X18_X55Y82	Multiplier location for Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X
Global Clocks:		
	GCLKBUF0 (or 1, 2, or 3)	Global clock buffer location for Spartan-II, Spartan-IIE, Virtex, Virtex-E
	GCLKPAD0 (or 1, 2, or 3)	Global clock pad location for Spartan-II, Spartan-IIE, Virtex, Virtex-E

Element Types	Location Examples	Meaning
Delay Locked Loops:		
	DLL0P(or S) (or 1, 2, or 3)	Delay Locked Loop element location for Spartan-II, Spartan-IIE, Virtex, Virtex-E
Digital Clock Manager:		
	DCM_X0Y0	Digital Clock Manager for Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X

The wildcard character (*) can be used to replace a single location with a range as shown in the following example:

CLB_R*C5	Any CLB in column 5 of a Spartan-II, Spartan-IIE, Virtex, or Virtex-E device
SLICE_X*Y5	Any slice of a Spartan-3, Virtex-II, Virtex-II Pro, or Virtex-II Pro X device whose Y coordinate is 5

The following are *not* supported.

- Dot extensions on ranges. For example, LOC=CLB_R0C0:CLB_R5C5.G.
- Wildcard character for Spartan-II, Spartan-IIE, Spartan-3, Virtex, Virtex-E, Virtex-II, Virtex-II Pro, or Virtex-II Pro X global buffer, global pad, or DLL locations.

LOC Priority

When specifying two adjacent LOCs on an input pad and its adjoining net, the LOC attached to the net has priority. In the following diagram, LOC=11 takes priority over LOC=38.

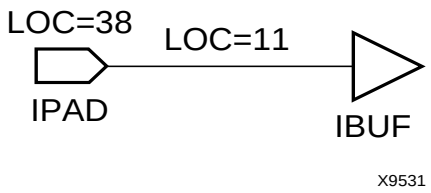


Figure 70-2: **LOC Priority Example**

LOC Propagation Rules

For all nets, LOC is illegal when attached to a net or signal except when the net or signal is connected to a pad. In this case, LOC is treated as attached to the pad instance.

For CPLD nets, LOC attaches to all applicable elements that drive the net or signal.

When attached to a design element, LOC propagates to all applicable elements in the hierarchy within the design element.

LOC Syntax for FPGAs

Single Location

The basic UCF syntax is:

```
INST "instance_name" LOC=location;
```

where *location* is a legal location for the part type.

Examples of the syntax for single LOC constraints are given in the following table.

Table 70-2: **Single LOC Constraint Examples**

Constraint (UCF Syntax)	Description
`INST "instance_name"LOC=P12;`	Place I/O at location P12.
`INST "instance_name"LOC=CLB_R3C5;` (Spartan-II, Spartan-IIE, Virtex, and Virtex-E)	Place logic in either slice of the CLB in row3, column 5.
`INST "instance_name"LOC=CLB_R3C5.S0;` (Spartan-II, Spartan-IIE, Virtex, and Virtex-E)	Place logic in the left slice of the CLB in row 3, column 5.
`INST "instance_name" LOC=SLICE_X3Y2;` (Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X)	Place logic in slice X3Y2 on the XY SLICE grid.
`INST "instance_name" LOC=TBUF_R1C2.*;` (Spartan-II, Spartan-IIE, Virtex, and Virtex-E)	Place both TBUFs in row 1, column 2.
`INST "instance_name" LOC=TBUF_X0Y6;` (Virtex-II, Virtex-II Pro, and Virtex-II Pro X)	Place logic in the BUFT located at TBUF_ X0Y6 on the XY SLICE grid
`INST "instance_name" LOC=RAMB4_R*C1;` (Spartan-II, Spartan-IIE, Virtex, and Virtex-E)	Specifies any block RAM in column 1 of the block RAM array

Table 70-2: **Single LOC Constraint Examples**

Constraint (UCF Syntax)	Description
`INST "instance_name" LOC=RAMB16_X0Y6;` (Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X)	Place the logic in the block RAM located at RAMB16_X0Y6 on the XY RAMB grid.
`INST "instance_name" LOC=MULT18X18_X0Y6;` (Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X)	Place the logic in the multiplier located at MULT18X18_X0Y6 on the XY MULT grid.

Multiple Locations

LOC=*location1*,*location2*,...,*locationx*

Separating each such constraint by a comma specifies multiple locations for an element. When you specify multiple locations, PAR can use any of the specified locations. Examples of multiple LOC constraints are provided in the following table.

Table 70-3: **Multiple LOC Constraint Examples**

Constraint	Description
`INST "instance_name" LOC=clb_r4c5.s1, clb_r4c6.*;` (Spartan-II, Spartan-IIE, Virtex, and Virtex-E)	Place the flip-flop in the right-most slice of CLB R4C5 or in either slice of CLB R4C6.
`INST "instance_name" LOC=SLICE_X2Y10, SLICE_X1Y10;` (Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X)	Place the logic in SLICE_X2Y10 or in SLICE_X1Y10 on the XY SLICE grid.

Currently, using a single constraint there is no way to constrain multiple elements to a single location or multiple elements to multiple locations.

Range of Locations

The basic UCF syntax is:

INST "*instance_name***" LOC=***location*:*location* [**SOFT**];

You can define a range by specifying the two corners of a bounding box. Except for Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X, specify the upper left and lower right corners of an area in which logic is to be placed. For Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X, specify the lower left and upper right corners. Use a colon (:) to separate the two boundaries.

The logic represented by the symbol is placed somewhere inside the bounding box. The default is to interpret the constraint as a “hard” requirement and to place it within the box. If SOFT is specified, PAR may place the constraint elsewhere if better results can be obtained at a location outside the bounding box. Examples of LOC constraints used to specify a range are given in the following table.

.

Table 70-4: **LOC Range Constraint Examples**

Constraint	Description
`INST “instance_name“ LOC=CLB_R1C1:CLB_R4C4;` (Spartan-II, Spartan-IIE, Virtex, and Virtex-E)	Place logic in either slice in the top left corner of the CLB bounded by row 4, column 4.
`INST “instance_name“ LOC=SLICE_X3Y5:SLICE_X5Y20;` (Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X)	Place logic in any slice within the rectangular area bounded by SLICE_X3Y5 (the lower left corner) and SLICE_X5Y20 (the upper right corner) on the XY SLICE grid.

LOC ranges can be supplemented with the keyword SOFT. Unlike AREA_GROUP, LOC ranges do not influence the packing of symbols. LOC range is strictly a placement constraint used by PAR.

LOC Syntax for CPLDs

The basic UCF syntax is:

INST “*instance_name***” LOC=***pin_name***;**

or

INST “*instance_name***” LOC=FB***ff***;**

or

INST “*instance_name***” LOC=FB***ff_mm***;**

where

- *pin_name* is P*nn* for numeric pin names or *rc* for row-column pin names.
- *ff* is a function block number.
- *mm* is a macrocell number within a function block.

LOC Syntax Examples

See the previous section and “RLOC” for multiple examples of legal placement constraints for each type of logic element (flip-flops, ROMs and RAMs, block RAMS, FMAPs, BUFTs, CLBs, IOBs, I/Os, edge decoders, global buffers) in FPGA designs.

Schematic

Attach to an instance.

Attribute Name—LOC

Attribute Values—*value*

See "LOC Syntax for FPGAs" and "LOC Syntax for CPLDs" for valid values.

VHDL

Before using LOC, declare it with the following syntax:

```
attribute loc: string;
```

After LOC has been declared, specify the VHDL constraint as follows:

```
attribute loc of {signal_name|label_name}: {signal|label} is
"location";
```

Furthermore, setting the LOC constraint on a bus is done as follows:

```
attribute loc of bus_name : signal is "location_1 location_2
location_3...";
```

To constrain only a portion of a bus (CPLDs only), use the following syntax:

```
attribute loc of bus_name : signal is "* * location_1 * location_2...";
```

See "LOC Syntax for FPGAs" and "LOC Syntax for CPLDs" for a description of *location*.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute loc [of] {instance_name|signal_name} [is]
location;
```

Furthermore, setting the LOC constraint on a bus is done as follows:

```
//synthesis attribute loc [of] bus_name [is] "location_1 location_2
location_3...";
```

To constrain only a portion of a bus (CPLDs only), use the following syntax:

```
//synthesis attribute loc [of] bus_name [is] "* * location_1 *
location_2...";
```

See "LOC Syntax for FPGAs" and "LOC Syntax for CPLDs" for a description of *location*.

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

- Pin Assignment

  ```
  mysignal PIN 12;
  ```

- Internal Location Constraint

  ```
  XILINX PROPERTY 'loc=fb1 mysignal';
  ```

UCF/NCF

- The following statement specifies that each instance found under "FLIP_FLOPS" is to be placed in any CLB in column 8.

  ```
  INST "/FLIP_FLOPS/*" LOC=CLB_R*C8;
  ```

- The following statement specifies that an instantiation of MUXBUF_D0_OUT be placed in IOB location P110.

  ```
  INST “MUXBUF_D0_OUT” LOC=P110;
  ```

- The following statement specifies that the net DATA<1> be connected to the pad from IOB location P111.

  ```
  NET “DATA<1>” LOC=P111
  ```

XCF

```
BEGIN MODEL “entity_name”
 PIN “signal_name”  loc=string;
 INST “instance_name” loc=string;
END;
```

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

In the Ports tab grid, double-click the Location column in the row with the desired port name and fill out the Location dialog box. This locks the selected signal to the specified pin. You cannot set any other location constraints in the Constraints Editor.

PCF

LOC writes out a LOCATE constraint to the PCF file. See “LOCATE”.

Floorplanner

After you place your logic within the Floorplanner, save the file as a UCF file to create a LOC constraint. See the following topics in the Floorplanner online help:

- Creating and Editing Area Constraints
- Using a Floorplanner UCF File in Project Navigator
- Assigning Area Constraints for Modular Design

PACE

The Pin Assignments Editor is mainly used for assigning location constraints to IOs in designs. You can access PACE from the Processes window in the Project Navigator. Double-click Assign Package Pins or Create Area Constraints under User Constraints.

For details on how to use PACE, see the PACE online help, especially the topics within Editing Pins and Areas in the Procedures section.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

BUFT Examples

You can constrain internal 3-state buffers (BUFTs) to an individual BUFT location, a list of BUFT locations, or a rectangular block of BUFT locations. BUFT constraints all refer to locations with a prefix of TBUF, which is the name of the physical element on the device.

BUFT constraints can be assigned from the schematic or through the UCF file. From the schematic, LOC constraints are attached to the target BUFT. The constraints are then passed into the EDIF netlist file and after mapping are read by PAR. Alternatively, in a constraints file a BUFT is identified by a unique instance name.

Virtex, Virtex-E, Spartan-II, and Spartan-IIE (Fixed Locations)

For Virtex, Virtex-E, Spartan-II, and Spartan-IIE use the following syntax to denote fixed locations.

TBUF_R*row***C***col***{.0|.1}**

where

- *row* is the row location
- *col* is the column location

They can be any number between 0 and 99, inclusive. They must be less than or equal to the number of CLB rows or columns in the target device.

A suffix of .0 or .1 is required.

The suffixes have the following meanings:

- 0 indicates at least one TBUF at the specific row / column
- 1 indicates the second TBUF at the specific row / column

Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X (Fixed Locations)

For Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X, use the following syntax to denote fixed locations:

TBUF_X*m***Y***n*

where *m* and *n* represent XY values on the slice-based X0Y0 grid.

The TBUFs are associated with the SLICE grid. Because there are two TBUFs per CLB and four slices per CLB, the X value for a TBUF location can only be an even integer or zero. The values must be less than or equal to the number of slices in the target device.

Spartan-II, Spartan-IIE, Virtex, and Virtex-E (Range of Locations)

For Spartan-II, Spartan-IIE, Virtex, or Virtex-E, use the following syntax to denote a range of locations from the lowest to the highest.

TBUF_R*row***C***col***:TBUF_R***row***C***col*

Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X (Range of Locations)

For Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X, use the following syntax to denote a range of locations from the lowest to the highest.

TBUF_X*value***Y***value***:TBUF_X***value***Y***value*

The following examples illustrate the format of BUFT LOC constraints. Specify LOC= and the BUFT location.

LOC=TBUF_R1C1.0 (or .1)	(Spartan-II, Spartan-IIE, Virtex, and Virtex-E)
LOC=TBUF_X2Y1	(Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X)

The next statements place BUFTs at any location in the first column of BUFTs. The asterisk (*) is a wildcard character.

LOC=TBUF_R*C0	(Spartan-II, Spartan-IIE, Virtex, and Virtex-E)
LOC=TBUF_X0Y*	(Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X)

The following statements place BUFTs within the rectangular block defined by the two TBUFs/LOCs. For all architectures except Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X, the first specified BUFT is in the upper left corner and the second specified BUFT is in the lower right corner. For Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X, the first BUFT is the lower left corner and the second is the upper right corner..

LOC=TBUF_R1C1:TBUF_R2C8	(Spartan-II, Spartan-IIE, Virtex, and Virtex-E)
LOC=TBUF_X0Y1:TBUF_X2Y8	(Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X)

Spartan-II, Spartan-IIE, Virtex, and Virtex-E (CLB-Based Row/Column/Slice Designations)

The examples in this section apply to the Spartan-II, Spartan-IIE, Virtex, and Virtex-E architectures.

In the following examples, the instance names of two BUFTs are /top-72/rd0 and /top-79/ed7.

Example 1

The following example specifies a BUFT adjacent to a specific CLB.

Schematic	LOC=TBUF_R1C5
UCF	INST “/top-72/rd0” LOC=TBUF_R1C5;

Place the BUFT adjacent to CLB R1C5. In Spartan-II, Spartan-IIE, Virtex, and Virtex-E, PAR places the BUFT in one of two slices of the CLB at row 1, column 5.

Example 2

The following example places a BUFT in a specific location.

Schematic	LOC=TBUF_r1c5.1
UCF	INST “/top-72/rd0” LOC=TBUF_r1c5.1;

Place the BUFT adjacent to CLB R1C5. In Spartan-II, Spartan-IIE, Virtex, and Virtex-E, the .1 tag specifies the second TBUF in CLB R1C5.

BUFTs that drive the same signal must carry consistent constraints. If you specify .1 or .2 for one of the BUFTs that drives a given signal, you must also specify .1 or .2 on the other BUFTs on that signal; otherwise, do not specify any constraints at all.

Example 3

The following example specifies a column of BUFTs.

Schematic	LOC=TBUF_r*c3
UCF	INST “/top-72/rd0 /top-79/ed7” LOC=TBUF_r*c3;

Place BUFTs in column 3 on any row. This constraint might be used to align BUFTs with a common enable signal. You can use the wildcard (*) character in place of either the row or column number to specify an entire row or column of BUFTs.

Example 4

The following example specifies a row of BUFTs.

Schematic	LOC=TBUF_r7c*
UCF	INST “/top-79/ed7” LOC=TBUF_r7c*;

Place the BUFT on one of the longlines in row 7 for any column. You can use the wildcard (*) character in place of either the row or column number to specify an entire row or column of BUFTs.

Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X (Sliced-Based XY Coordinate Designations)

The examples in this section apply to the Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X architectures.

Example 1

The following example places a BUFT in a specific location.

Schematic	LOC=TBUF_X4Y5
UCF	INST “/top-72/rd0” LOC=TBUF_X4Y5;

Place the BUFT in TBUF_X4Y5 in the CLB containing SLICE_X4Y5.

BUFTs that drive the same signal must carry consistent constraints.

Example 2

The following example specifies a column of BUFTs.

Schematic	LOC=TBUF_X6Y*
UCF	INST “/top-72/rd0 /top-79/ed7” LOC=TBUF_X6Y*;

Place BUFTs in the column of CLBs that contains the TBUFs whose X coordinate is 6. This constraint might be used to align BUFTs with a common enable signal. You can use the wildcard (*) character in place of either the X or Y coordinate to specify an entire row (X*) or column (Y*) of BUFTs.

Example 3

The following example specifies a row of BUFTs.

Schematic	LOC=TBUF_X*Y6
UCF	INST “/top-79/ed7” LOC=TBUF_X*Y6;

Place the BUFT on one of the longlines in the row of CLBs that contains TBUFs whose Y coordinate is 6. You can use the wildcard (*) character in place of either the X or Y coordinate to specify an entire row (X*) or column (Y*) of TBUFs.

CLB Examples (CLB-Based Row/Column/Slice Architectures Only)

Note: This section applies only to the architecture that uses the CLB-based Row/Column/Slice designations:

You can assign soft macros and flip-flops to a single CLB location, a list of CLB locations, or a rectangular block of CLB locations. You can also specify the exact function generator or flip-flop within a CLB. CLB locations are identified as CLB_R*row*C*col* for Spartan-II, Spartan-IIE, Virtex, and Virtex-E. The upper left CLB is CLB_R1C1.

CLB Locations

CLB locations can be a fixed location or a range of locations.

Fixed Locations

Use the following syntax to denote fixed locations.

For Spartan-II, Spartan-IIE, Virtex, and Virtex-E:

CLB_R*row***C***col*{**.S0 | .S1**}

where

- *row* is the row location
- *col* is the column location

They can be any number between 0 and 99, inclusive, or *.

They must be less than or equal to the number of CLB rows or columns in the target device.

The suffixes have the following meanings.

- .S0 means the right-most slice in the Spartan-II, Spartan-IIE, Virtex, and Virtex-E CLB
- .S1 means the left-most slice in the Spartan-II, Spartan-IIE, Virtex, and Virtex-E CLB

Range of Locations

Use the following syntax to denote a range of locations from the highest to the lowest.

CLB_R*row1***C***col***:CLB_R***row2***C***col2*

Format of CLB Constraints

The following examples illustrate the format of CLB constraints. Enter LOC= and the pin or CLB location. If the target symbol represents a soft macro, the LOC constraint is applied to all appropriate symbols (flip-flops, maps) contained in that macro. If the indicated logic does not fit into the specified blocks, an error is generated.

- The following UCF statement places logic in the designated CLB.

  INST "*instance_name***" LOC=CLB_R1C1.S0;**

  (Spartan-II, Spartan-IIE, Virtex, and Virtex-E)

- The following UCF statement places logic within the first column of CLBs. The asterisk (*) is a wildcard character.

  INST "*instance_name***" LOC=CLB_R*C1.S0;**

  (Spartan-II, Spartan-IIE, Virtex, and Virtex-E)

- The next two UCF statements place logic in any of the three designated CLBs. There is no significance to the order of the LOC statements.

  INST "*instance_name***" LOC=CLB_R1C1,CLB_R1C2,CLB_R1C3;**

  (Spartan-II, Spartan-IIE, Virtex, and Virtex-E)

- The following statement places logic within the rectangular block defined by the first specified CLB in the upper left corner and the second specified CLB towards the lower right corner.

  INST "*instance_name***" LOC=CLB_R1C1:CLB_R8C5;**

  (Spartan-II, Spartan-IIE, Virtex, and Virtex-E)

You can prohibit PAR from using a specific CLB, a range of CLBs, or a row or column of CLBs. Such PROHIBIT constraints can be assigned only through the User Constraints File (UCF). CLBs are prohibited by specifying a PROHIBIT constraint at the design level, as shown in the following examples.

Example 1

Do not place any logic in the CLB in row 1, column 5. CLB R1C1 is in the upper left corner of the device.

Schematic	None
UCF	CONFIG PROHIBIT=clb_r1c5;

Example 2

Do not place any logic in the rectangular area bounded by the CLB R1C1 in the upper left corner and CLB R5C7 in the lower right.

Schematic	None
UCF	CONFIG PROHIBIT=clb_r1c1:clb_r5c7;

Example 3

Do not place any logic in any row of column 3. You can use the wildcard (*) character in place of either the row or column number to specify an entire row or column of CLBs.

Schematic	None
UCF	CONFIG PROHIBIT=clb_r*c3;

Example 4

Do not place any logic in either CLB R2C4 or CLB R7C9.

Schematic	None
UCF	CONFIG PROHIBIT=clb_r2c4, clb_r7c9;

Delay Locked Loop (DLL) Constraint Examples (Spartan-II, Spartan-IIE, Virtex, and Virtex-E Only)

You can constrain DLL elements—CLKDLL, CLKDLLE, and CLKDLLHF—to a specific physical site name. Specify LOC=DLL and a numeric value (0 through 3) to identify the location.

Following is an example.

Schematic	LOC=DLL1P
UCF	INST “buf1” LOC=DLL1P;

Digital Clock Manager (DCM) Constraint Examples (Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X Only)

You can lock the DCM in the UCF file:

The syntax is as follows:

```
INST “instance_name” LOC = DCM_XAYB;
```

A is the X coordinate, starting with 0 at the left-hand bottom corner. *A* increases in value as you move across the device to the right.

B is the Y coordinate, starting with 0 at the left-hand bottom corner. *B* increases in value as you move up the device.

For example:

```
INST “myinstance” LOC = DCM_X0Y0;
```

Flip-Flop Constraint Examples

Flip-flop constraints can be assigned from the schematic or through the UCF file.

From the schematic, attach LOC constraints to the target flip-flop. The constraints are then passed into the EDIF netlist and are read by PAR after the design is mapped.

The following examples show how the LOC constraint is applied to a schematic and to a UCF (User Constraints File). The instance names of two flip-flops, /top-12/fdrd and /top-54/fdsd, are used to show how you would enter the constraints in the UCF.

CLB-Based Row/Column/Slice Designations

The Virtex architecture uses CLB-based Row/Column/Slice designations:

Flip-flops can be constrained to a specific CLB, a range of CLBs, a row or column of CLBs, or a specific half-CLB.

Example 1

Place the flip-flop in the CLB in row 1, column 5. CLB R1C1 is in the upper left corner of the device.

Schematic	LOC=CLB_RlC5
UCF	INST "/top-12/fdrd" LOC=CLB_R1C5;

Example 2

Place the flip-flop in the rectangular area bounded by the CLB R1C1 in the upper left corner and CLB R5C7 in the lower right corner.

Schematic	LOC=CLB_R1C1:CLB_R5C7
UCF	INST "/top-12/fdrd" LOC=CLB_R1C1:CLB_R5C7;

Example 3

Place the flip-flops in any row of column 3. You can use the wildcard (*) character in place of either the row or column number to specify an entire row or column of CLBs.

Schematic	LOC=CLB_R*C3
UCF	INST "/top-12/fdrd/top-54/fdsd" LOC=CLB_R*C3;

Example 4

Place the flip-flop in either CLB R2C4 or CLB R7C9.

Schematic	LOC=CLB_R2C4,CLB_R7C9
UCF	INST "/top-54/fdsd" LOC=CLB_R2C4,CLB_R7C9;

In Example 4, repeating the LOC constraint and separating each such constraint by a comma specifies multiple locations for an element. When you specify multiple locations, PAR can use any of the specified locations.

Example 5

Do not place the flip-flop in any column of row 5. You can use the wildcard (*) character in place of either the row or column number to specify an entire row or column of CLBs.

Schematic	PROHIBIT=CLB_R5C*
UCF	CONFIG PROHIBIT=CLB_R5C*;

Slice-Based XY Grid Designations

Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X are the only architectures that use slice-based XY grid designations.

Flip-flops can be constrained to a specific slice, a range of slices, a row or column of slices.

Example 1

Place the flip-flop in SLICE_X1Y5. SLICE_X0Y0 is in the lower left corner of the device.

Schematic	LOC=SLICE_XlY5
UCF	INST “/top-12/fdrd” LOC=SLICE_X1Y5;

Example 2

Place the flip-flop in the rectangular area bounded by the SLICE_X1Y1 in the lower left corner and SLICE_X5Y7 in the upper right corner.

Schematic	LOC=SLICE_R1C1:SLICE_R5C7
UCF	INST “/top-12/fdrd” LOC=SLICE_X1Y1:SLICE_X5Y7;

Example 3

Place the flip-flops anywhere in the row of slices whose Y coordinate is 3. Use the wildcard (*) character in place of either the X or Y value to specify an entire row (Y*) or column (X*) of slices.

Schematic	LOC=SLICE_X*Y3
UCF	INST “/top-12/fdrd/top-54/fdsd” LOC=SLICE_X*Y3;

Example 4

Place the flip-flop in either SLICE_X2Y4 or SLICE_X7Y9.

Schematic	LOC=SLICE_X2Y4,SLICE_X7Y9
UCF	INST “/top-54/fdsd” LOC=SLICE_X2Y4, SLICE_X7Y9;

In Example 4, repeating the LOC constraint and separating each such constraint by a comma specifies multiple locations for an element. When you specify multiple locations, PAR can use any of the specified locations.

Example 5

Do not place the flip-flop in the column of slices whose X coordinate is 5. Use the wildcard (*) character in place of either the X or Y value to specify an entire row (Y*) or column (X*) of slices.

Schematic	PROHIBIT=SLICE_X5Y*
UCF	CONFIG PROHIBIT=SLICE_X5Y*;

Global Buffer Constraint Examples

This section provides global buffer constraint examples for Spartan-II, Spartan-IIE, Spartan-3, Virtex, Virtex-E, Virtex-II, Virtex-II Pro, and Virtex-II Pro X.

You can constrain a Spartan-II, Spartan-IIE, Spartan-3, Virtex, Virtex-E, Virtex-II, Virtex-II Pro, and Virtex-II Pro X global buffer—BUFGP, and IBUFG_SelectIO variants—to a specific buffer site name or dedicated global clock pad in the device model. From the schematic, attach LOC constraints to the global buffer symbols. Specify LOC= and GCLKBUF plus a number (0 through 3) to create a specific buffer site name in the device model. Or, specify LOC= and GCLKPAD plus a number (0 through 3) to create a specific dedicated global clock pad in the device model. The constraints are then passed into the EDIF netlist and after mapping are read by PAR.

Example

Schematic	LOC=GCLKBUF1
UCF	INST “buf1” LOC=GCLKBUF1;
Schematic	LOC=GCLKPAD1
UCF	INST “buf1” LOC=GCLKPAD1;

I/O Constraint Examples

You can constrain I/Os to a specific IOB. You can assign I/O constraints from the schematic or through the UCF file.

From the schematic, attach LOC constraints to the target PAD symbol. The constraints are then passed into the netlist file and read by PAR after mapping.

Alternatively, in the UCF file a pad is identified by a unique instance name. The following example shows how the LOC constraint is applied to a schematic and to a UCF (User Constraints File). In the examples, the instance names of the I/Os are /top-102/data0_pad and /top-117/q13_pad. The example uses a pin number to lock to one pin.

Schematic	LOC=P17
UCF	INST “/top-102/data0_pad” LOC=P17;

Place the I/O in the IOB at pin 17. For pin grid arrays, a pin name such as B3 or T1 is used.

IOB Constraint Examples

You can assign I/O pads, buffers, and registers to an individual IOB location. IOB locations are identified by the corresponding package pin designation.

The following examples illustrate the format of IOB constraints. Specify LOC= and the pin location. If the target symbol represents a soft macro containing only I/O elements, for example, INFF8, the LOC constraint is applied to all I/O elements contained in that macro. If the indicated I/O elements do not fit into the specified locations, an error is generated.

The following UCF statement places the I/O element in location P13. For PGA packages, the letter-number designation is used, for example, B3.

```
INST "instance_name" LOC=P13;
```

You can prohibit the mapper from using a specific IOB. You might take this step to keep user I/O signals away from semi-dedicated configuration pins. Such PROHIBIT constraints can be assigned only through the UCF file.

IOBs are prohibited by specifying a PROHIBIT constraint preceded by the CONFIG keyword, as shown in the following example.

Schematic	None
UCF	CONFIG PROHIBIT=p36, p37, p41;

Do not place user I/Os in the IOBs at pins 36, 37, or 41. For pin grid arrays, pin names such as D14, C16, or H15 are used.

Mapping Constraint Examples (FMAP)

Mapping constraints control the mapping of logic into CLBs. They have two parts. The first part is an FMAP component placed on the schematic. The second is a LOC constraint that can be placed on the schematic or in the constraints file.

FMAP controls the mapping of logic into function generators. This symbol does not define logic on the schematic; instead, it specifies how portions of logic shown elsewhere on the schematic should be mapped into a function generator.

The FMAP symbol defines mapping into a four-input (F) function generator. For Spartan-II, Spartan-IIE, Virtex, and Virtex-E, the four-input function generator defined by the FMAP is assigned to one of the two slices of the CLB.

For the FMAP symbol as with the CLBMAP primitive, MAP=PUC or PUO is supported, as well as the LOC constraint. (Currently, pin locking is not supported. MAP=PLC or PLO is translated into PUC and PUO, respectively.)

Example 1

Place the FMAP symbol in the CLB at row 7, column 3.

Schematic	LOC=CLB_R7C3
UCF	INST "$1I323" LOC=CLB_R7C3;

Example 2

Place the FMAP symbol in either the CLB at row 2, column 4 or the CLB at row 3, column 4.

Schematic	LOC=CLB_R2C4,CLB_R3C4
UCF	INST “top / dec0011” LOC=CLB_R2C4,CLB_R3C4;

Example 3

Place the FMAP symbol in the area bounded by CLB R5C5 in the upper left corner and CLB R10C8 in the lower right

Schematic	LOC=CLB_R5C5:CLB_R10C8
UCF	INST “$3I27” LOC=CLB_R5C5:CLB_R10C8;

Example 4 (Virtex, Virtex-E, Spartan-II, and Spartan-IIE)

Place the FMAP in the right-most slice of the CLB in row 10, column 11.

Schematic	LOC=CLB_R10C11.S0
UCF	INST “ / top / done” LOC=CLB_R10C11.S0;

Multiplier Constraint Examples (Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X Only)

Multiplier constraints can be assigned from the schematic or through the UCF file. From the schematic, attach the LOC constraints to a multiplier symbol. The constraints are then passed into the netlist file and after mapping they are read by PAR. For more information on attaching LOC constraints, see the appropriate interface user guide. Alternatively, in the constraints file a multiplier is identified by a unique instance name.

A Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X multiplier has a different XY grid specification than slices, block RAMs, and TBUFs. It is specified using MULT18X18_X*m*Y*n* where the X and Y coordinate values correspond to the multiplier grid array. A multiplier located at MULT18X18_X0Y1 is not located at the same site as a flip-flop located at SLICE_X0Y1 or a block RAM located at RAMB16_X0Y1.

For example, assume you have a device with two columns of multipliers, each column containing two multipliers, where one column is on the right side of the chip and the other is on the left. The multiplier located in the lower left corner is MULT18X18_X0Y0. Because there are only two columns of multipliers, the multiplier located in the upper right corner is MULT18X18_X1Y1.

Schematic	LOC=MULT18X18_X0Y0
UCF	INST “ / top-7 / rq” LOC=MULT18X18_X0Y0;

ROM Constraint Examples

Memory constraints can be assigned from the schematic or through the UCF file.

From the schematic, attach the LOC constraints to the memory symbol. The constraints are then passed into the netlist file and after mapping they are read by PAR. For more information on attaching LOC constraints, see the appropriate interface user guide.

Alternatively, in the constraints file memory is identified by a unique instance name. One or more memory instances of type ROM can be found in the input file. All memory macros larger than 16 x 1 or 32 x 1 are broken down into these basic elements in the netlist file.

In the following examples, the instance name of the ROM primitive is /top-7/rq.

CLB-Based Row/Column/Slice Designations

The Virtex architecture uses CLB-based Row/Column/Slice designations:

You can constrain a ROM to a specific CLB, a range of CLBs, a row or column of CLBs.

Example 1

Place the memory in the CLB in row 1, column 5. CLB R1C1 is in the upper left corner of the device. You can only apply a single-CLB constraint such as this to a 16 x 1 or 32 x 1 memory.

Schematic	LOC=clb_r1c5
UCF	INST "/top-7/rq" LOC=clb_r1c5;

Example 2

Place the memory in either CLB R2C4 or CLB R7C9.

Schematic	LOC=clb_r2c4, clb_r7c9
UCF	INST "/top-7/rq" LOC=clb_r2c4, clb_r7c9;

Example 3

Do not place the memory in any column of row 5. You can use the wildcard (*) character in place of either the row or column number in the CLB name to specify an entire row or column of CLBs.

Schematic	PROHIBIT clb_r5c*
UCF	CONFIG PROHIBIT=clb_r5c*;

Slice-Based XY Designations

Currently only Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X use slice-based XY grid designations.

You can constrain a ROM to a specific slice, a range of slices, or a row or column of slices.

Example 1

Place the memory in the SLICE_X1Y1. SLICE_X1Y1 is in the lower left corner of the device. You can only apply a single-SLICE constraint such as this to a 16 x 1 or 32 x 1 memory.

Schematic	LOC=SLICE_X1Y1
UCF	INST “/top-7/rq” LOC=SLICE_X1Y1;

Example 2

Place the memory in either SLICE_X2Y4 or SLICE_X7Y9.

Schematic	LOC=SLICE_X2Y4, SLICE_X7Y9
UCF	INST “/top-7/rq” LOC=SLICE_X2Y4, SLICE_X7Y9;

Example 3

Do not place the memory in column of slices whose X coordinate is 5. You can use the wildcard (*) character in place of either the X or Y coordinate value in the SLICE name to specify an entire row (Y*) or column (X*) of slices.

Schematic	PROHIBIT SLICE_X5Y*
UCF	CONFIG PROHIBIT=SLICE_X5Y*;

Block RAM (RAMBs) Constraint Examples (Spartan-II, Spartan-IIE, Spartan-3, Virtex, Virtex-E, Virtex-II, Virtex-II Pro, and Virtex-II Pro X)

Block RAM constraints can be assigned from the schematic or through the UCF file. From the schematic, attach the LOC constraints to the block RAM symbol. The constraints are then passed into the netlist file. After mapping they are read by PAR. For more information on attaching LOC constraints, see the appropriate interface user guide. Alternatively, in the constraints file a memory is identified by a unique instance name.

Spartan-II, Spartan-IIE, Virtex, and Virtex-E

A Spartan-II, Spartan-IIE, Virtex, and Virtex-E block RAM has a different row/column grid specification than CLBs and TBUFs. It is specified using RAMB4_RnCn where the numeric row and column numbers refer to the block RAM grid array. A block RAM located at RAMB4_R3C1 is not located at the same site as a flip-flop located at CLB_R3C1.

For example, assume you have a device with two columns of block RAM, each column containing four blocks, where one column is on the right side of the chip and the other is on the left. The block RAM located in the upper left corner is RAMB4_R0C0. Because there are only two columns of block RAM, the block located in the upper right corner is RAMB4_R0C1.

Schematic	LOC=RAMB4_R0C0
UCF	INST “/top-7/rq” LOC=RAMB4_R0C0;

Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X

A Spartan-3, Virtex-II, Virtex-II Pro, or Virtex-II Pro X block RAM has a different XY grid specification than a slice, multiplier, or TBUF. It is specified using RAMB16_X*m*Y*n* where the X and Y coordinate values correspond to the block RAM grid array. A block RAM located at RAMB16_X0Y1 is not located at the same site as a flip-flop located at SLICE_X0Y1.

For example, assume you have a device with two columns of block RAM, each column containing two blocks, where one column is on the right side of the chip and the other is on the left. The block RAM located in the lower left corner is RAMB16_X0Y0. Because there are only two columns of block RAM, the block located in the upper right corner is RAMB16_X1Y1.

Schematic	LOC=RAMB16_X0Y0
UCF	INST “/top-7/rq” LOC=RAMB16_X0Y0;

Slice Constraint Examples (Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X Only)

Note: This section applies only to Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X. These are currently the only architectures that use the slice-based XY grid designations.

You can assign soft macros and flip-flops to a single slice location, a list of slice locations, or a rectangular block of slice locations.

Slice locations can be a fixed location or a range of locations. Use the following syntax to denote fixed locations.

SLICE_X*m*Y*n*

where *m* and *n* are the X and Y coordinate values, respectively.

They must be less than or equal to the number of slices in the target device.

Use the following syntax to denote a range of locations from the highest to the lowest.

SLICE_X*m*Y*n*:SLICE_X*m*Y*n*

Examples (Format of Slice Constraints)

The following examples illustrate the format of slice constraints: LOC= and the slice location. If the target symbol represents a soft macro, the LOC constraint is applied to all appropriate symbols (flip-flops, maps) contained in that macro. If the indicated logic does not fit into the specified blocks, an error is generated.

Example 1

The following UCF statement places logic in the designated slice for Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X.

```
INST “instance_name” LOC=SLICE_X133Y10;
```

Example 2

The following UCF statement places logic within the first column of slices for Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X. The asterisk (*) is a wildcard character.

```
INST “instance_name” LOC=SLICE_X0Y*;
```

Example 3

The following UCF statement places logic in any of the three designated slices for Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X. There is no significance to the order of the LOC statements.

```
INST "instance_name" LOC=SLICE_X0Y3, SLICE_X67Y120, SLICE_X3Y0;
```

Example 4

For Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X, the following UCF statement places logic within the rectangular block defined by the first specified slice in the lower left corner and the second specified slice towards the upper right corner.

```
INST "instance_name" LOC=SLICE_X3Y22:SLICE_X10Y55;
```

Examples (Slices Prohibited)

You can prohibit PAR from using a specific slice, a range of slices, or a row or column of slices. Such prohibit constraints can be assigned only through the User Constraints File (UCF). Slices are prohibited by specifying a PROHIBIT constraint at the design level, as shown in the following examples.

Example 1

Do not place any logic in the SLICE_X0Y0. SLICE_X0Y0 is at the lower left corner of the device.

Schematic	None
UCF	CONFIG PROHIBIT=SLICE_X0Y0;

Example 2

Do not place any logic in the rectangular area bounded by SLICE_X2Y3 in the lower left corner and SLICE_X10Y10 in the upper right.

Schematic	None
UCF	CONFIG PROHIBIT=SLICE_X2Y3:SLICE_X10Y10;

Example 3

Do not place any logic in a slice whose location has 3 as the X coordinate. This designates a column of prohibited slices. You can use the wildcard (*) character in place of either the X or Y coordinate to specify an entire row (X*) or column (Y*) of slices.

Schematic	None
UCF	CONFIG PROHIBIT=SLICE_X3Y*;

Example 4

Do not place any logic in either SLICE_X2Y4 or SLICE_ X7Y9.

Schematic	None
UCF	CONFIG PROHIBIT=SLICE_X2Y4, SLICE_X7Y9;

LOC for Modular Designs

The PIN / LOC UCF constraint has the following syntax:

```
PIN "module.pin" LOC="location";
```

This UCF syntax is only used within the modular design flow. This constraint is translated into a COMP / LOCATE constraint in the PCF file. This constraint has the following syntax:

```
COMP "name" LOCATE = SITE "location";
```

The PIN / LOC constraint specifies that the pseudo component that will be created for pin “pin” on module “module” should be located in the site location. Pseudo logic is only created when a net connects from a pin on one module to a pin on another module.

LOCATE

LOCATE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

LOCATE Applicable Elements

CLBs, IOBs, TBUFs, DCMs, clock logic, macros

LOCATE Description

LOCATE is a basic placement constraint and a modular design constraint. It specifies a single location, multiple single locations, or a location range.

LOCATE Propagation Rules

When attached to a macro, the constraint propagates to all elements of the macro. When attached to a primitive, the constraint applies to the entire primitive.

LOCATE Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Single or multiple single locations

COMP “*comp_name*” **LOCATE=**[**SOFT**] “*site_item1*”. . . “*site_itemn*” [**LEVEL** *n*];
COMPGRP “*group_name*” **LOCATE=**[**SOFT**] “*site_item1*”. . . “*site_itemn*” [**LEVEL** *n*];
MACRO *name* **LOCATE=**[**SOFT**] “*site_item1*”. . . “*site_itemn*” [**LEVEL** *n*];

Range of locations

COMP “*comp_name*” **LOCATE=**[**SOFT**] **SITE** “*site_name*” **:** **SITE** “*site_name*” [**LEVEL** *n*];
COMPGRP “*group_name*” **LOCATE=**[**SOFT**] **SITE** “*site_name*” **:** **SITE** “*site_name*” [**LEVEL** *n*];
MACRO “*macro_name*” **LOCATE=**[**SOFT**] **SITE** “*site_name*” **:** **SITE** “*site_name*” [**LEVEL** *n*];

where

- *site_name* is a component site (that is, a CLB or IOB location)
- *site_item* is one of the following
  - **SITE** “*site_name*”
  - **SITEGRP** “*site_group_name*”
- *n* in LEVEL n is 0, 1, 2, 3, or 4.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

LOCATE for Modular Design Use

The AREA_GROUP / RANGE constraint is translated into a COMPGRP / LOCATE constraint in the PCF file. This constraint has the following syntax:

```
COMPGRP "name" LOCATE = SITE "start:end";
```

See “AREA_GROUP -- Modular Design Use”.

The PIN / LOC constraint is translated into a COMP / LOCATE constraint in the PCF file. This constraint has the following syntax:

```
COMP "name" LOCATE = SITE "location";
```

See “LOC for Modular Designs”.

LOCK

LOCK Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

LOCK Applicable Elements

Nets

LOCK Description

LOCK is an advanced routing constraint. It locks a net that has been previously placed or routed (that is, cannot be unplaced, unrouted, moved, swapped, or deleted). LOCK can also be used to lock all nets.

LOCK Propagation Rules

Applies to the nets to which it is assigned.

LOCK Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

LOCK_PINS

LOCK_PINS Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

LOCK_PINS Applicable Elements

The LOCK_PINS constraint is only applied to specific instances of LUT symbols.

LOCK_PINS Description

The LOCK_PINS constraint instructs the implementation tools to not swap the pins of the LUT symbol to which it is attached. The LOCK_PINS constraint should not be confused with the Lock Pins process in Project Navigator, which is used to preserve the existing pinout of a CPLD design.

LOCK_PINS Propagation Rules

LOCK_PINS is only applied to a single LUT instance.

LOCK_PINS Syntax Examples

Schematic

Not applicable.

VHDL

Before using LOCK_PINS, declare it with the following syntax:

```
attribute lock_pins: string;
```

After LOCK_PINS has been declared, specify the VHDL constraint as follows:

```
attribute lock_pins of {component_name|label_name } : {component|label}
is "true";
```

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

```
//synthesis attribute LOCK_PINS [of] {module_name|instance name} [is]
true;
```

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

```
INST "XSYM1" LOCK_PINS;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

LUT_MAP

LUT_MAP Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

LUT_MAP Applicable Elements

LUT_MAP can be applied to a VHDL entity or Verilog module.

LUT_MAP Description

Using the UNISIM library allows you to directly instantiate LUT components in your HDL code. To specify a function that a particular LUT must execute, apply an INIT constraint to the instance of the LUT. If you want to place an instantiated LUT or register in a particular slice, then attach an RLOC constraint to the same instance.

It is not always convenient to calculate INIT functions and different methods can be used to achieve this. Instead, you can describe the function that you want to map onto a single LUT in your VHDL or Verilog code in a separate block. Attaching a LUT_MAP constraint (XST is able to automatically recognize the XC_MAP constraint supported by Synplicity) to this block will indicate to XST that this block must be mapped on a single LUT. XST will

automatically calculate the INIT value for the LUT and preserve this LUT during optimization.

Please refer to "Specifying INITs and RLOCs in HDL Code" section in the *XST User Guide* for more details.

LUT_MAP Propagation Rules

Applies to the entity or module to which it is attached.

LUT_MAP Syntax Examples

Schematic

Not applicable.

VHDL

Before using LUT_MAP, declare it with the following syntax:

```
attribute lut_map: string;
```

After LUT_MAP has been declared, specify the VHDL constraint as follows:

```
attribute lut_map of entity_name : entity is “yes”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute lut_map [of] module_name [is] “yes”;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

XCF

```
MODEL “entity_name” lut_map={yes|true};
```

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

MAP

MAP Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

MAP Applicable Elements

FMAP

MAP Description

MAP is an advanced mapping constraint. Place MAP on an FMAP to specify whether pin swapping and the merging of other functions with the logic in the map are allowed. If merging with other functions is allowed, other logic can also be placed within the CLB, if space allows.

MAP Propagation Rules

Applies to the design element to which it is attached.

MAP Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name" MAP=[PUC | PUO | PLC | PLO];
```

where the terms have the following meanings:

- PUC
  The CLB pins are unlocked (U) and the CLB is closed (C).
- PUO
  The CLB pins are unlocked (U) and the CLB is open (O).
- PLC
  The CLB pins are locked (L) and the CLB is closed (C).
- PLO
  The CLB pins are locked (L) and the CLB is open (O).

The default is PUO. Currently, only PUC and PUO are observed. PLC and PLO are translated into PUC and PUO, respectively.

As used in these definitions, the following terms have the meanings indicated.

- Unlocked
  The software can swap signals among the pins on the CLB.
- Locked
  The software *cannot* swap signals among the pins on the CLB.
- Open
  The software can add or remove logic from the CLB.
- Closed
  The software *cannot* add or remove logic from the function specified by the MAP symbol.

The following statement allows pin swapping and ensures that no logic other than that defined by the original map will be mapped into the function generators.

```
INST "$1I3245/map_of_the_world" map=puc;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

MAX_FANOUT

MAX_FANOUT Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

MAX_FANOUT Applicable Elements

You can apply MAX_FANOUT globally or to a VHDL entity, a Verilog module, or signal.

MAX_FANOUT Description

MAX_FANOUT is a synthesis constraint. It limits the fanout of nets or signals. The constraint value is an integer, and the default is 100 for Virtex, Virtex-E, Spartan-II, and Spartan-IIE; and 500 for Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4. It is both a global and a local constraint.

Large fanouts can cause routability problems, therefore XST tries to limit fanout by duplicating gates or by inserting buffers. This limit is not a technology limit but a guide to XST. It may happen that this limit is not exactly respected, especially when this limit is small (below 30).

In most cases, fanout control is performed by duplicating the gate driving the net with a large fanout. If the duplication cannot be performed, then buffers will be inserted. These

buffers will be protected against logic trimming at the implementation level by defining a **KEEP** attribute in the NGC file.

If the register replication option is set to NO, only buffers are used to control fanout of flip-flops and latches.

MAX_FANOUT is global for the design, but you can control maximum fanout independently for each entity or module or for given individual signals by using constraints.

If the actual net fanout is less than MAX_FANOUT value, then XST behavior depends on the way the MAX_FANOUT is specified.

- If MAX_FANOUT value is set via Project Navigator, in command line or attached to a specific hierarchical block, then XST interprets its value as a guidance.
- If MAX_FANOUT is attached to a specific net, then XST does not perform logic replication. Please note that putting MAX_FANOUT on the net may prevent XST from having better timing optimization.

For example, suppose that the critical path goes through the net, which actual fanout is 80 and set MAX_FANOUT value to 100. If MAX_FANOUT is specified via Project Navigator, then XST may replicate it, trying to improve timing. If MAX_FANOUT is attached to the net itself, then XST will not perform logic replication.

MAX_FANOUT Propagation Rules

Applies to the entity, module, or signal to which it is attached.

MAX_FANOUT Syntax Examples

Schematic

Not applicable.

VHDL

Before using MAX_FANOUT, declare it with the following syntax:

```
attribute MAX_FANOUT: string;
```

After MAX_FANOUT has been declared, specify the VHDL constraint as follows:

```
attribute MAX_FANOUT of {signal_name|entity_name}: {signal|entity} is
“integer”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
 // synthesis attribute MAX_FANOUT [of] {signal_name|module_name } [is]
integer;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL "entity_name" max_fanout=integer;

BEGIN MODEL "entity_name"
 NET "signal_name" max_fanout=integer;
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-MAX_FANOUT** command line option of the **run** command. Following is the basic syntax:

```
-MAX_FANOUT integer
```

The default value of integer is 100 for Virtex /E, Spartan-II/IIE. It is 500 for Spartan-3, Virtex-II/II Pro/II Pro X.

Project Navigator

Set globally with the Max Fanout option in the Xilinx Specific Options tab in Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

MAXDELAY

MAXDELAY Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

MAXDELAY Applicable Elements

Nets

MAXDELAY Description

The MAXDELAY attribute defines the maximum allowable delay on a net.

MAXDELAY Propagation Rules

Applies to the net to which it is attached.

MAXDELAY Syntax Examples

Schematic

Attach to a net.

Attribute Name— MAXDELAY

Attribute Values—*value units*

value is the numerical time delay.

units are us, ms, ns, ps.

VHDL

Before using MAXDELAY, declare it with the following syntax:

```
attribute maxdelay: string;
```

After MAXDELAY has been declared, specify the VHDL constraint as follows:

```
attribute maxdelay of signal_name: signal is "value [units]";
```

where *value* is a positive integer.

Valid units are ps, ns, us, ms, GHz, MHz, and kHz. The default is ns.

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
// synthesis attribute maxdelay [of] signal_name [is] value [units];
```

where *value* is a positive integer.

Valid units are ps, ns, us, ms, GHz, MHz, and kHz. The default is ns.

For a more detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

```
NET "net_name" MAXDELAY=value units;
```

value is the numerical time delay.

units are us, ns, ms, ps.

The following statement assigns a maximum delay of 1 us to the net $SIG_4.

```
NET "$1I3245/$SIG_4" MAXDELAY=10 ns;
```

XCF

Not yet supported.

Constraints Editor

Not applicable.

PCF

```
item MAXDELAY = maxvalue [PRIORITY integer];
```

where *item* can be:

- **ALLNETS**
- **NET** *name*
- **TIMEGRP** *name*
- **ALLPATHS**
- **PATH** *name*
- *path specification*

maxvalue can be:

- a numerical time value with units of us, ms, ps, or ns
- a numerical frequency value with units of GHz, MHz, or KHz
- a TSidentifier

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

To set MAXDELAY to all paths or nets, click Main Properties from the File menu and select the Global Physical Constraints tab..

To set the constraint to a selected path or net, click Properties of Selected Items from the Edit menu with a routed net selected and use the Physical Constraints tab.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

MAXPT

MAXPT Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	No
Spartan-3E	No
Virtex-II	No
Virtex-II Pro	No
Virtex-II Pro X	No
Virtex-4	No
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

MAXPT Applicable Elements

Signals

MAXPT Description

MAXPT is an advanced ABEL constraint. It applies to CPLDs only. MAXPT specifies the maximum number of product terms the fitter is permitted to use when collapsing logic into the node to which MAXPT is applied. MAXPT overrides the Collapsing P-term Limit setting in Project Navigator for the attached node.

MAXPT Propagation Rules

Applies to the signal to which it is attached.

MAXPT Syntax Examples

Schematic

Not applicable.

VHDL

Before using MAXPT, declare it with the following syntax:

```
attribute maxpt: integer;
```

After MAXPT has been declared, specify the VHDL constraint as follows:

```
attribute maxpt of signal_name : signal is “integer”;
```

where *integer* is any positive integer.

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute maxpt [of] signal_name [is] integer;
```

where *integer* is any positive integer.

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

```
XILINX PROPERTY 'maxpt=8 mysignal';
```

Valid values are any positive integers.

UCF/NCF

```
Net “signal_name” maxpt=integer;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

MAXSKEW

MAXSKEW Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

MAXSKEW Applicable Elements

Nets

MAXSKEW Description

MAXSKEW is an advanced timing constraint. Skew is the difference between the load delays on a net. You can control the maximum allowable skew on a net by attaching

MAXSKEW directly to the net. It is important to understand exactly what MAXSKEW defines. Consider the following example.

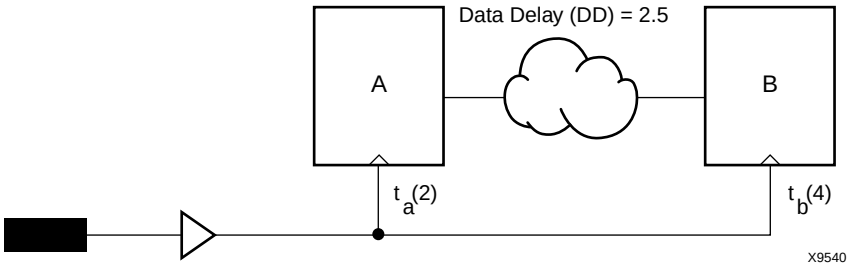


Figure 79-1: **MAXSKEW**

In the preceding diagram, for $t_a(2)$, 2 ns is the maximum delay for the Register A clock. For $t_b(4)$, 4 ns is the maximum delay for the Register B clock. MAXSKEW defines the maximum of t_b minus the maximum of t_a, that is, 4-2=2.

Overuse of this constraint, or too tight of a requirement (value), can cause long PAR runtimes.

MAXSKEW Propagation Rules

Applies to the net to which it is attached.

MAXSKEW Syntax Examples

Schematic

Attach to a net.

Attribute Name—MAXSKEW

Attribute Values—*allowable_skew* [*units*]

where

- *allowable_skew* is the timing requirement
- *units* may be ms, us, ns, ps. The default is ns.

VHDL

Before using MAXSKEW, declare it with the following syntax:

```
attribute maxskew: string;
```

After MAXSKEW has been declared, specify the VHDL constraint as follows:

```
attribute maxskew of signal_name : signal is "allowable_skew [units]";
```

where *allowable_skew* is the timing requirement.

Valid *units* are ps, ns, us, ms, GHz, MHz, and kHz. The default is ns.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
// synthesis attribute maxskew [of] signal_name [is] allowable_skew
[units];
```

where *allowable_skew* is the timing requirement.

Valid *units* are ps, ns, us, ms, GHz, MHz, and kHz. The default is ns.

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

```
NET "net_name" MAXSKEW=allowable_skew [units];
```

where

- *allowable_skew* is the timing requirement
- *units* may be ms, us, ns, ps. The default is ns.

The following statement specifies a maximum skew of 3 ns on net $SIG_6.

```
NET "$1I3245/$SIG_6" MAXSKEW=3 ns;
```

XCF

Not yet supported.

Constraints Editor

Not applicable.

PCF

Same as UCF.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

To set constraints, in the FPGA Editor main window, click Properties of Selected Items from the Edit menu. With a routed net selected, you can set MAXSKEW from the Physical Constraints tab.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

MOVE_FIRST_STAGE

MOVE_FIRST_STAGE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

MOVE_FIRST_STAGE Applicable Elements

These two constraints can be applied only to the following:

- entire design
- single modules or entities
- primary clock signal

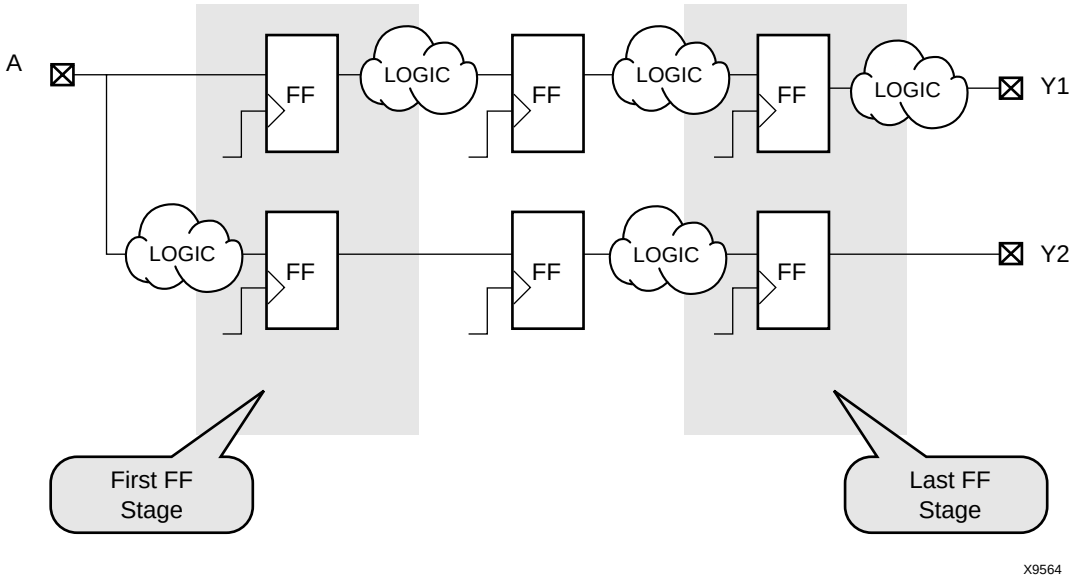
MOVE_FIRST_STAGE Description

This constraint as well as MOVE_LAST_STAGE are synthesis constraints that directly relate to the Register Balancing process.

Definitions:

- A flip-flop (FF in the diagram) belongs to the First Stage if it is on the paths coming from primary inputs.

- An FF belongs to the Last Stage if it is on the paths going to primary outputs.



During the register balancing process FFs belonging to the First Stage will be moved forward and FFs, belonging to the last stage will be moved backward. This process can dramatically increase input-to-clock and clock-to-output timing, which is not desirable. To prevent this, you may use OFFSET_IN_BEFORE and OFFSET_IN_AFTER constraints.

In the case:

- The design does not have a strong requirements, or
- You would like to see the first results without touching the first and last FF stages

Two additional constraints can be used: MOVE_FIRST_STAGE and MOVE_LAST_STAGE. Both constraints may have 2 values: **yes** and **no**.

- MOVE_FIRST_STAGE=no will prevent the first FF stage from movement.
- MOVE_LAST_STAGE=no will prevent the last FF stage from movement.

MOVE_FIRST_STAGE Propagation Rules

See "MOVE_FIRST_STAGE Description".

MOVE_FIRST_STAGE Syntax Examples

Schematic

Not applicable.

VHDL

Before using MOVE_FIRST_STAGE, declare it with the following syntax:

```
attribute move_first_stage : string;
```

After MOVE_FIRST_STAGE has been declared, specify the VHDL constraint as follows:

```
attribute move_first_stage of {entity_name|signal_name}:
{signal|entity} is “yes”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute move_first_stage [of] {module_name|signal_name}
[is] yes;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL “entity_name” move_first_stage={yes|no|true|false};


BEGIN MODEL “entity_name”
 NET “primary_clock_signal”  move_first_stage={yes|no|true|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-move_first_stage** command line option of the **run** command. Following is the basic syntax:

```
-move_first_stage {YES|NO}
```

The default is **YES**.

Project Navigator

Set with the Move First Flip-Flop Stage option in the Xilinx Specific Options tab of the Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

MOVE_LAST_STAGE

MOVE_LAST_STAGE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

MOVE_LAST_STAGE Applicable Elements

These two constraints can be applied only to the following:

- entire design
- single modules or entities
- primary clock signal

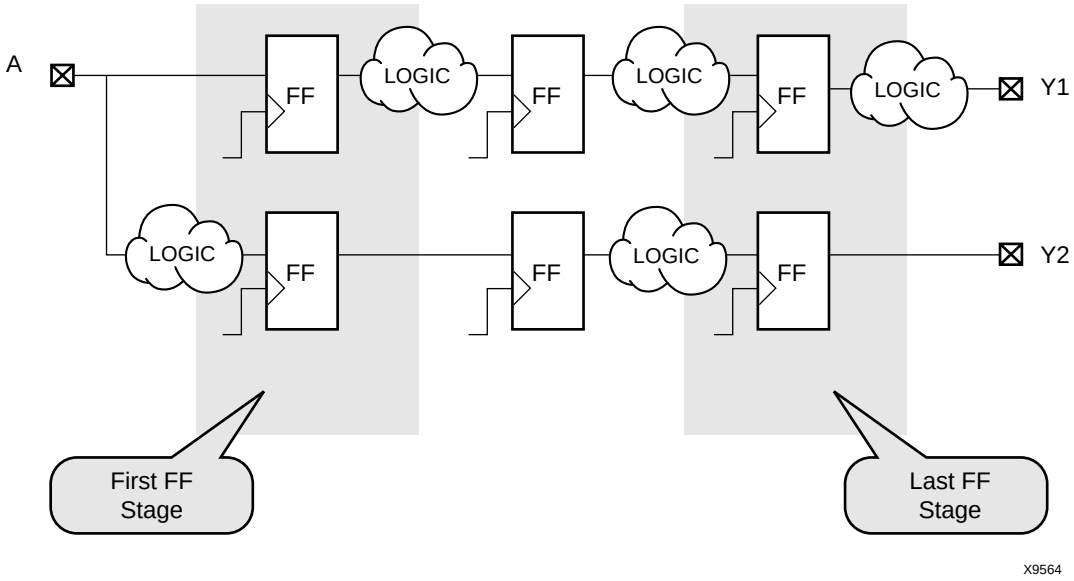
MOVE_LAST_STAGE Description

This constraint as well as MOVE_FIRST_STAGE are synthesis constraints that directly relate to the Register Balancing process.

Definitions:

- A flip-flop (FF in the diagram) belongs to the First Stage if it is on the paths coming from primary inputs.

- A FF belongs to the Last Stage if it is on the paths going to primary outputs.



During the register balancing process FFs belonging to the First Stage will be moved forward and FFs, belonging to the last stage will be moved backward. This process can dramatically increase input-to-clock and clock-to-output timing, which is not desirable. To prevent this, you may use OFFSET_IN_BEFORE and OFFSET_IN_AFTER constraints.

In the case:

- The design does not have a strong requirements, or
- You would like to see the first results without touching the first and last FF stages

Two additional constraints can be used: MOVE_FIRST_STAGE and MOVE_LAST_STAGE. Both constraints may have two values: **yes** and **no**.

- MOVE_FIRST_STAGE=no will prevent the first FF stage from movement.
- MOVE_LAST_STAGE=no will prevent the last FF stage from movement.

MOVE_LAST_STAGE Propagation Rules

See “MOVE_LAST_STAGE Description”.

MOVE_LAST_STAGE Syntax Examples

Schematic

Not applicable.

VHDL

Before using MOVE_LAST_STAGE, declare it with the following syntax:

```
attribute move_last_stage : string;
```

After MOVE_LAST_STAGE has been declared, specify the VHDL constraint as follows:

```
attribute move_last_stage of {entity_name|signal_name}:
{signal|entity} is “yes”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute move_last_stage [of] {module_name|signal_name}
[is] yes;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL “entity_name” move_last_stage={{yes|no|true|false};

BEGIN MODEL “entity_name”
 NET “primary_clock_signal”  move_last_stage={yes|no|true|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-move_last_stage** command line option of the **run** command. Following is the basic syntax:

```
-move_last_stage {YES|NO}
```

The default is **YES**.

Project Navigator

Set with the Move Last Flip-Flop Stage option in the Xilinx Specific Options tab of the Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

MULT_STYLE

MULT_STYLE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

MULT_STYLE Applicable Elements

MULT_STYLE can be applied globally or to a VHDL entity, a Verilog module, or signal.

MULT_STYLE Description

This is a synthesis constraint. This constraint controls the way the macrogenerator implements the multiplier macros. Allowed values are **auto**, **block**, **lut**, **pipe_block**, **KCM**, **CSD**, and **pipe_lut**. Please note that pipe_block value is supported for Virtex4 family only. For Virtex, Virtex-E, Spartan-II, and Spartan-IIE, the default is **lut**, meaning that XST looks for the best implementation for each considered macro. For Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4, the default is **auto**.

The **pipe_lut** option is for pipeline slice-based multipliers. See the Release Notes for more information. The implementation style can be manually forced to use block multiplier or LUT resources available in Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4 devices.

The pipe_block option is to pipeline DSP48 based multipliers and available for Virtex-4 family only.

MULT_STYLE Propagation Rules

Applies to the entity, module, or signal to which it is attached.

MULT_STYLE Syntax Examples

Schematic

Not applicable.

VHDL

Before using MULT_STYLE, declare it with the following syntax:

```
attribute mult_style: string;
```

After MULT_STYLE has been declared, specify the VHDL constraint as follows:

```
attribute mult_style of {signal_name|entity_name}: {signal|entity} is
"{auto|block|lut|pipe_lut|pipe_block|CSD|KCM}";
```

For Virtex, Virtex-E, Spartan-II, and Spartan-IIE, the default is **lut**. For Virtex-II, Virtex-II Pro, Virtex-II Pro X, Virtex-4, and Spartan-3, the default is **auto**.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
// synthesis attribute mult_style [of] {module_name|signal_name} [is]
{auto|block|lut|pipe_lut|pipe_block|CSD|KCM};
```

For Virtex, Virtex-E, Spartan-II, and Spartan-IIE, the default is **lut**. For Virtex-II, Virtex-II Pro, Virtex-II Pro X, Virtex-4, and Spartan-3, the default is **auto**.

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

NCF

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL "entity_name"
mult_style={auto|block|lut|pipe_lut|pipe_block|CSD|KCM};
```

```
BEGIN MODEL "entity_name"
 NET "signal_name"
mult_style={auto|block|lut|pipe_lut|pipe_block|CSD|KCM};
END;
```

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-mult_style** command line option of the **run** command. Following is the basic syntax:

```
-mult_style {AUTO|BLOCK|LUT|PIPE_LUT|PIPE_BLOCK|KCM}
```

For Virtex, Virtex-E, Spartan-II, and Spartan-IIE, the default is **lut**. For Virtex-II, Virtex-II Pro, Virtex-II Pro X, Virtex-4, and Spartan-3, the default is **auto**.

Project Navigator

Set globally with the Multiplier Style property in the HDL Options tab of the Process Properties dialog box within the Project Navigator. With a source file selected in the Sources in Project window, right-click Synthesize in the Processes for Source window to access the appropriate Process Properties dialog box.

MUX_EXTRACT

MUX_EXTRACT Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

MUX_EXTRACT Applicable Elements

You can apply MUX_EXTRACT globally or to a VHDL entity, a Verilog module, or signal.

MUX_EXTRACT Description

MUX_EXTRACT is a synthesis constraint. It enables or disables multiplexer macro inference. Allowed values are YES, NO and FORCE (TRUE and FALSE ones are available in XCF as well).

By default, multiplexer inference is enabled (**YES**). For each identified multiplexer description, based on some internal decision rules, XST actually creates a macro or optimizes it with the rest of the logic. The **FORCE** value allows you to override those decision rules and force XST to create the MUX macro.

MUX_EXTRACT Propagation Rules

Applies to the entity, module, or signal to which it is attached.

MUX_EXTRACT Syntax Examples

Schematic

Not applicable.

VHDL

Before using MUX_EXTRACT, declare it with the following syntax:

```
attribute mux_extract: string;
```

After MUX_EXTRACT has been declared, specify the VHDL constraint as follows:

```
attribute mux_extract of {signal_name|entity_name}: {entity|signal} is
"{yes|no|force}";
```

The default value is **YES**.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
// synthesis attribute mux_extract [of] {module_name|signal_name} [is]
{yes|no|force};
```

The default value is **YES**.

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL "entity_name" mux_extract={yes|no|force|true|false};

BEGIN MODEL "entity_name"
 NET "signal_name" mux_extract={yes|no|force|true|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-mux_extract** command line option of the **run** command. Following is the basic syntax:

```
-mux_extract {YES|NO|FORCE}
```

The default value is **YES**.

Project Navigator

Set MUX_EXTRACT globally with the Mux Extraction option in the HDL Options tab of the Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

MUX_STYLE

MUX_STYLE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

MUX_STYLE Applicable Elements

MUX_STYLE can be applied globally or to a VHDL entity, a Verilog module, or signal.

MUX_STYLE Description

MUX_STYLE is a synthesis constraint. It controls the way the macrogenerator implements the multiplexer macros. Allowed values are auto, muxf and muxcy. The default value is auto, meaning that XST looks for the best implementation for each considered macro. Available implementation styles for the Virtex, Virtex-E, and Spartan-II, Spartan-IIE series are based on either MUXF5 and MUXF6 resources, or MUXCY resources. In addition, Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4 can use MUXF7, and MUXF8 resources as well.

MUX_STYLE Propagation Rules

Applies to the entity, module, or signal to which it is attached.

MUX_STYLE Syntax Examples

Schematic

Not applicable.

VHDL

Before using MUX_STYLE, declare it with the following syntax:

```
attribute mux_style: string;
```

After MUX_STYLE has been declared, specify the VHDL constraint as follows:

```
attribute mux_style of {signal_name|entity_name}: {signal|entity} is
"{auto|muxf|muxcy}";
```

The default value is **AUTO.**

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute mux_style [of] {module_name|signal_name} [is]
{auto|muxf|muxcy};
```

The default value is **AUTO.**

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL "entity_name" mux_style={auto|muxf|muxcy};

BEGIN MODEL "entity_name"
 NET "signal_name" mux_style={auto|muxf|muxcy};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-mux_style** command line option of the **run** command. Following is the basic syntax:

```
-mux_style {AUTO|MUXF|MUXCY}
```

The default is **AUTO**.

Project Navigator

Set globally with the Mux Style option in the HDL Options tab of the Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

NODELAY

NODELAY Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

NODELAY Applicable Elements

Input register

You can also attach NODELAY to a net connected to a pad component in a UCF file. NGDBuild transfers the constraint from the net to the pad instance in the NGD file so that it can be processed by the mapper. Use the following UCF syntax:

```
NET "net_name" NODELAY;
```

NODELAY Description

NODELAY is an advanced mapping constraint. The default configuration of IOB flip-flops in designs includes an input delay that results in no external hold time on the input data path. This delay can be removed by placing NODELAY on input flip-flops or latches, resulting in a smaller setup time but a positive hold time.

The input delay element is active in the default configuration for Spartan-II, Spartan-3, Virtex, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4.

NODELAY can be attached to the I/O symbols and the special function access symbols TDI, TMS, and TCK.

NODELAY Propagation Rules

NODELAY is illegal when attached to a net or signal except when the net or signal is connected to a pad. In this case, NODELAY is treated as attached to the pad instance.

When attached to a design element, NODELAY is propagated to all applicable elements in the hierarchy within the design element.

NODELAY Syntax Examples

Schematic

Attach to a valid instance.

Attribute Name—NODELAY

Attribute Values—TRUE, FALSE

VHDL

Before using NODELAY, declare it with the following syntax:

```
attribute nodelay: string;
```

After NODELAY has been declared, specify the VHDL constraint as follows:

```
attribute nodelay of {component_name|signal_name|label_name}:
{component|signal|label} is "true";
```

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute nodelay [of]
{module_name|instance_name|signal_name} [is] true;
```

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

The following statement specifies that IOB register inreg67 not have an input delay.

```
INST "$1I87/inreg67" NODELAY;
```

The following statement specifies that there be no input delay to the pad that is attached to net1.

```
NET "net1" NODELAY;
```

XCF

```
BEGIN MODEL “entity_name”
 NET  "signal_name" nodelay=true;
 INST "instance_name" nodelay=true;
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

NOREDUCE

NOREDUCE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	No
Spartan-3E	No
Virtex-II	No
Virtex-II Pro	No
Virtex-II Pro X	No
Virtex-4	No
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

NOREDUCE Applicable Elements

Any net

NOREDUCE Description

NOREDUCE is a fitter and synthesis constraint. It prevents minimization of redundant logic terms that are typically included in a design to avoid logic hazards or race conditions. NOREDUCE also identifies the output node of a combinatorial feedback loop to ensure correct mapping. When constructing combinatorial feedback latches in a design, always apply NOREDUCE to the latch's output net and include redundant logic terms when necessary to avoid race conditions.

NOREDUCE Propagation Rules

NOREDUCE is a net or signal constraint. Any attachment to a design element is illegal.

NOREDUCE Syntax Examples

Schematic

Attach to a net.

Attribute Name—NOREDUCE

Attribute Values—TRUE, FALSE

VHDL

Before using NOREDUCE, declare it with the following syntax:

```
attribute noreduce: string;
```

After NOREDUCE has been declared, specify the VHDL constraint as follows:

```
attribute noreduce of signal_name: signal is “yes”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute noreduce [of] signal_name [is] “yes”;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

```
mysignal NODE istype 'retain’;
```

UCF/NCF

The following statement specifies that there be no Boolean logic reduction or logic collapse from the net named $SIG_12 forward.

```
NET “$SIG_12” NOREDUCE;
```

XCF

```
BEGIN MODEL “entity_name”
 NET “signal_name” noreduce={yes|no|true|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

OFFSET

OFFSET Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

OFFSET Applicable Elements

Global, nets, time groups

OFFSET Description

OFFSET is a basic timing constraint. It specifies the timing relationship between an external clock and its associated data-in or data-out pin. OFFSET is used only for pad-related signals, and cannot be used to extend the arrival time specification method to the internal signals in a design. A clock that comes from an internal signal is one generated from a synch element, like a FF. A clock that comes from a PAD and goes through a DLL, DCM, clock buffer, or combinatorial logic is supported.

Uses of OFFSET

OFFSET allows you to:

- Calculate whether a setup time is being violated at a flip-flop whose data and clock inputs are derived from external nets.
- Specify the delay of an external output net derived from the Q output of an internal flip-flop being clocked from an external device pin.

Advantages of OFFSET

Following are some of the advantages of OFFSET over a FROM:TO constraint:

- Includes the clock path delay for each individual synchronous element
- Includes clock phase introduced by a DLL / DCM for each individual synchronous element
- Includes clock phase introduced by a rising or falling clock edge
- Subtracts the clock path delay from the data path delay for inputs and adds the clock path delay to the data path delay for outputs
- Checks for hold time violations on inputs
- Includes paths for all synchronous element types (FFS, RAMS, CPUs, MULTS, HSIOS, and LATCHES)
- Utilizes a global syntax that allows all inputs or outputs to be constrained by a clock
- Allows specifying IO constraints either directly as the setup and clock-to-out required by a device (IN BEFORE and OUT AFTER) or indirectly as the time used by the path external to the device (IN AFTER and OUT BEFORE)

Types of Offset Specifications

There are basically three types of offset specifications:

- Global
- Net-specific
- Group

For CPLD designs, clock inputs referenced by OFFSET constraints must be explicitly assigned to a global clock pin (using either the BUFG symbol or applying the BUFG=CLK constraint to an ordinary input). Otherwise, OFFSET will not be used during timing-driven optimization of the design.

OFFSET Propagation Rules

OFFSET is a net constraint. Any attachment to a design element is illegal.

OFFSET Syntax

Global Method

UCF Syntax

```
OFFSET = {IN|OUT} “offset_time” [units] [VALID <datavalid time>]
{BEFORE|AFTER} “clk_name” [TIMEGRP “group_name”];
```

PCF Syntax

```
OFFSET = {IN|OUT} "offset_time" [units] [VALID <datavalid time>]
{BEFORE|AFTER} COMP "clk_iob_name" [TIMEGRP "group_name"];[HIGH/LOW]
```

where

- *offset_time* is the external differential between the initial clock edge and data transition. The initial clock edge is defined by the period constraint keyword HIGH / LOW or the HIGH / LOW keyword on the OFFSET constraint.
- *units* is an optional field that indicates the units for the offset time. The default units are nanoseconds, but the timing number can be followed by ps, ns, us, ms to show the intended units.
- The UCF syntax variable *clk_name* is the fully hierarchical net name of the clock net between its pad and its input buffer.
- The PCF syntax variable *clk_iob_name* is the block name of the clock IOB.
- The optional TIMEGRP *group_name* defines a group of registers that will be analyzed. By default, all registers clocked by *clk_name* will be analyzed.
- **IN** | **OUT** specifies that the offset is computed with respect to an input IOB or an output IOB. For a bidirectional IOB, the **IN** | **OUT** syntax lets you specify the flow of data (input or output) on the IOB.
- **BEFORE** | **AFTER** describe data arrival in relation to the current clock or the next clock edge.

  BEFORE defines the relationship between data arrival and the next clock edge. For example, OFFSET IN BEFORE indicates that data will be valid at the input pin of a Xilinx device at a specified time before the next clock edge arrives at the Xilinx device.

  AFTER defines the relationship between data arrival and the current clock edge. For example, OFFSET IN AFTER indicates that data will be valid at the input of a Xilinx device at a specified amount of time AFTER the current clock edge on the upstream device.
- All inputs / outputs are offset relative to *clk_name* or *clk_iob_name*. For example, **OFFSET= IN 20 ns BEFORE clk1** dictates that all inputs will have data present at the pad at least 20 ns before the initial edge of clk1 arrives at the pad.
- VALID defines how long the data will be valid. By default, it is equal to the offset time, which specifies a zero hold time requirement. If the data is available after the clock edge, use the VALID keyword to define the entire data valid window. VALID must be larger or equal to the offset time. Please see "Source Synchronous Timing" for more information.
- HIGH / LOW can be used to override the HIGH / LOW keyword defined on the PERIOD constraint. This is useful for DDR designs when one signal is captured by a rising or falling clock edge FF for setup or created by a rising or falling clock edge FF for CLOCK-TO-OUT. Please see "Source Synchronous Timing" for more information.

Net-Specific Method

OFFSET can also be used to specify a constraint for a specific data net in a UCF file or schematic or a specific input or output component in a PCF file.

Schematic Syntax When Attached to a Net

```
OFFSET = {IN|OUT} "offset_time" [units] {BEFORE|AFTER} "clk_name"
[TIMEGRP "group_name"]
```

UCF Syntax

```
 NET "pad_net_name" OFFSET = {IN|OUT} "offset_time" [units]
{BEFORE|AFTER} "clk_name" [TIMEGRP "group_name"];
```

PCF Syntax

```
 COMP "pad_net_name" OFFSET = {IN|OUT} "offset_time" [units]
{BEFORE|AFTER} COMP "clk_iob_name" [TIMEGRP "group_name"];
```

where

- *pad_net_name* is the name of the net attached to the pad.
- *offset_time* is the external differential between the initial clock edge and data transition.
- *units* is an optional field that indicates the units for offset time. The default units are in nanoseconds, but the timing number can be followed by ps, ns, us to indicate the intended units.
- *clk_iob_name* is the block name of the clock IOB

The PCF file uses IO blocks (comps) instead of nets.

If **COMP** "iob_name" is omitted in the PCF or NET "name" is omitted in the UCF, the specification is assumed to be global.

It is possible for one offset constraint to generate multiple data and clock paths (for example, when both data and clock inputs have more than a single sequential element in common).

OFFSET Examples

The OFFSET examples in this section apply to the following figures.

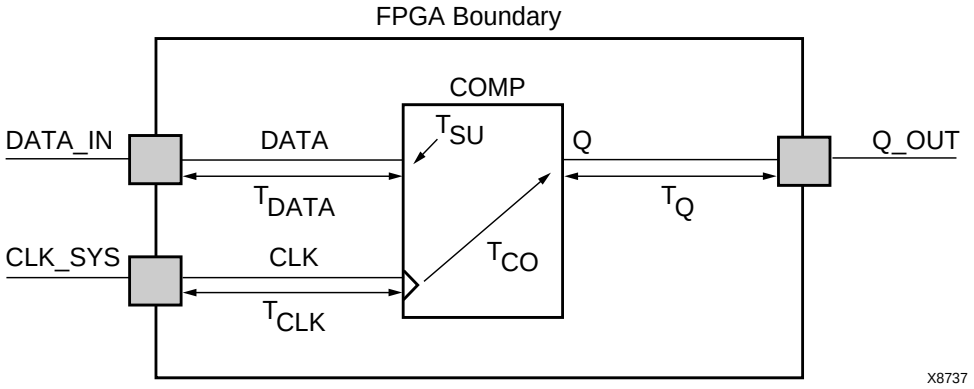


Figure 87-1: **OFFSET Example Schematic**

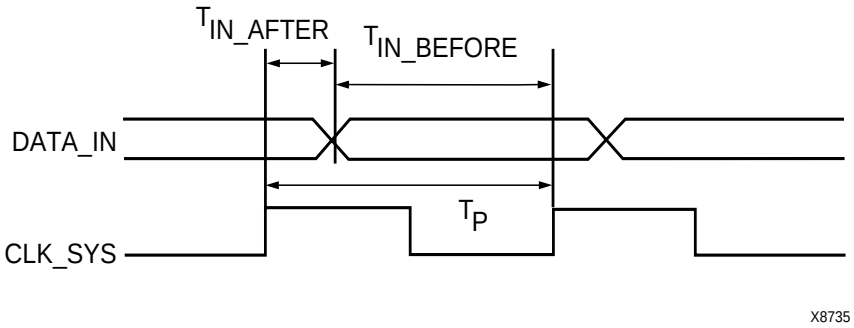


Figure 87-2: **OFFSET IN Timing Diagram**

Example 1— OFFSET IN BEFORE

OFFSET IN BEFORE defines the available time for data to propagate from the pad and setup at the synchronous element (COMP). The time can be thought of as the time differential of data arriving at the edge of the device before the next clock edge arrives at the device. See Figure 87-1 and Figure 87-2. The equation that defines this relationship is as follows.

$$T_{DATA} + T_{SU} - T_{CLK} \leq T_{IN\_BEFORE}$$

For example, if T_{IN_BEFORE} equals 20 ns, the following syntax applies.

Schematic syntax attached to DATA_IN

```
OFFSET=IN 20.0 BEFORE “CLK_SYS”
```

UCF syntax

```
NET “DATA_IN” OFFSET=IN 20.0 BEFORE “CLK_SYS”;
```

PCF syntax

```
COMP “DATA_IN” OFFSET=IN 20.0 ns BEFORE COMP “CLK_SYS”;
```

This constraint indicates that the data will be present on the DATA_IN pad at least 20 ns before the triggering edge of the clock net arrives at the clock pad.

To ensure that the timing requirements are met, the timing analysis software verifies that the maximum delay along the path DATAIN to COMP (minus the 20.0 ns offset) would be less than or equal to the minimum delay along the reference path CLOCK to COMP.

Example 2 — OFFSET IN AFTER

This constraint describes the time used by the data external to the FPGA. OFFSET subtracts this time from the PERIOD declared for the clock to determine the available time for the data to propagate from the pad and setup at the synchronous element. The time can be thought of as the differential of data arriving at the edge of the device after the current clock edge arrives at the edge of the device. See Figure 87-1 and Figure 87-2. The equation that defines this relationship is as follows.

$$T_{DATA} + T_{SU} - T_{CLK} \leq T_P - T_{IN\_AFTER}$$

T_P is the clock period.

For example, if T_{IN_AFTER} equals 30 ns, the following syntax applies.

Schematic syntax attached to DATA_IN

```
OFFSET=IN 30.0 AFTER “CLK_SYS”
```

UCF syntax

```
NET “DATA_IN” OFFSET=IN 30.0 AFTER “CLK_SYS”;
```

PCF syntax

```
COMP “DATA_IN” OFFSET=IN 30.0 ns AFTER COMP “CLK_SYS”;
```

This constraint indicates that the data will arrive at the pad of the device (COMP) no more than 30 ns after the triggering edge of the clock arrives at the clock pad. The path DATA_IN to COMP would contain the setup time for the COMP data input relative to the CLK_SYS input.

Verification is almost identical to Example 1, except that the offset margin (30.0 ns) is added to the data path delay. This is caused by the data arriving after the reference input. The timing analysis software verifies that the data can be clocked in prior to the next triggering edge of the clock.

A PERIOD or FREQUENCY is required only for offset **OUT** constraints with the **BEFORE** keyword, or for offset **IN** with the **AFTER** keyword.

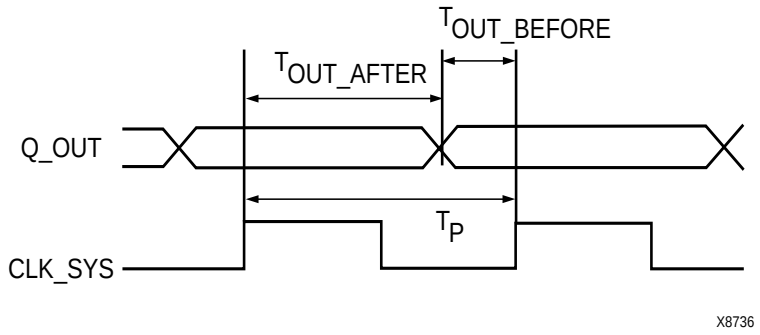


Figure 87-3: **OFFSET OUT Timing Diagram**

Example 3 — OFFSET OUT AFTER

This constraint defines the time available for the data to propagate from the synchronous element to the pad. This time can also be considered as the differential of data leaving the edge of the device after the current clock edge arrives at the edge of the device. See Figure 87-1 and Figure 87-3.

The equation that defines this relationship is as follows.

$$T_Q + T_{CO} + T_{CLK} \leq T_{OUT\_AFTER}$$

For example, if T_{OUT_AFTER} equals 35 ns, the following syntax applies.

Schematic syntax attached to Q_OUT

```
OFFSET=OUT 35.0 AFTER "CLK_SYS"
```

UCF syntax

```
NET "Q_OUT" OFFSET=OUT 35.0 AFTER "CLK_SYS";
```

PCF syntax

```
COMP "Q_OUT" OFFSET=OUT 35.0 ns AFTER COMP "CLK_SYS";
```

This constraint calls for the data to leave the FPGA 35 ns after the present clock input arrives at the clock pad. The path COMP to Q_OUT would include the CLOCK-to-Q delay (component delay).

Verification involves ensuring that the maximum delay along the reference path (CLK_SYS to COMP) and the maximum delay along the data path (COMP to Q_OUT) does not exceed the specified offset.

Example 4 — OFFSET OUT BEFORE

This constraint defines the time used by the data external to the FPGA. OFFSET subtracts this time from the clock PERIOD to determine the available time for the data to propagate from the synchronous element to the pad. The time can also be considered as the differential of data leaving the edge of the device before the next clock edge arrives at the edge of the device. See Figure 87-1 and Figure 87-3. The equation that defines this relationship is as follows.

$$T_Q + T_{CO} + T_{CLK} \leq T_P - T_{OUT\_BEFORE}$$

For example, if T_{OUT_BEFORE} equals 15 ns, the following syntax applies.

Schematic syntax attached to Q_OUT

```
OFFSET=OUT 15.0 BEFORE “CLK_SYS”
```

UCF syntax

```
NET “Q_OUT” OFFSET=OUT 15.0 BEFORE “CLK_SYS”;
```

PCF syntax

```
COMP “Q_OUT” OFFSET=OUT 15.0 ns BEFORE COMP “CLK_SYS”;
```

This constraint states that the data clocked to Q_OUT must leave the FPGA 15 ns before the next triggering edge of the clock arrives at the clock pad. The path COMP to Q_OUT includes the CLK_SYS-to-Q delay (component delay). The data clocked to Q_OUT will leave the FPGA 15.0 ns before the next clock input.

Verification involves ensuring that the maximum delay along the reference path (CLK_SYS to COMP) and the maximum delay along the data path (COMP to Q_OUT) do not exceed the clock period minus the specified offset.

As in Example 2, a PERIOD or FREQUENCY constraint is required only for offset OUT constraints with the BEFORE keyword, or for offset IN with the AFTER keyword.

Input/Output Group Method

It is better to group inputs and outputs into a single timegrp when they have the same timing requirement. This will reduce place and route runtime, static timing runtime, memory usage, and will generate a smaller report.

```
TIMEGRP “name” OFFSET={IN | OUT} offset_time [units] {BEFORE | AFTER}
"clk_net" [TIMEGRP "reggroup"];
```

where

- *group* is the name of a time group containing IOB components (UCF) or pad BELs (PCF)
- *offset_time* is the external offset
- *units* is an optional field to indicate the units for the offset time. The default is nanoseconds, but the timing number can be followed by ps, ns, us, ms, GHz, MHz, or kHz to indicate the intended units.
- IN or OUT specifies that the offset is computed with respect to an input IOB or an output IOB. For a bidirectional IOB, the IN or OUT lets you specify the flow of data (input output) on the IOB.
- BEFORE or AFTER indicates whether the data is to arrive (input) or leave (output) the device before or after the clock input
- *clk_net* is the fully hierarchical netname of the clock net between the pad and its input buffer. All inputs / outputs are offset relative to clk_net
- *reggroup* previously defined time group of register BELs

Valid HIGH/LOW

Only registers in the time group clocked by the specified IOB component is checked against the specified offset time. The optional time group qualifier, TIMEGRP "reggroup," can be added to any OFFSET constraint to indicate that the offset applies only to registers specified in the qualifying group. When used with the "Register Group method," the

"register time" group lists the synchronous elements that qualify which register elements clocked by "clk_net" get analyzed.

Register Group Method

A clock register time group allows you to define a specific set of registers to which an OFFSET constraint applies based on a clock edge. Consider the following example.

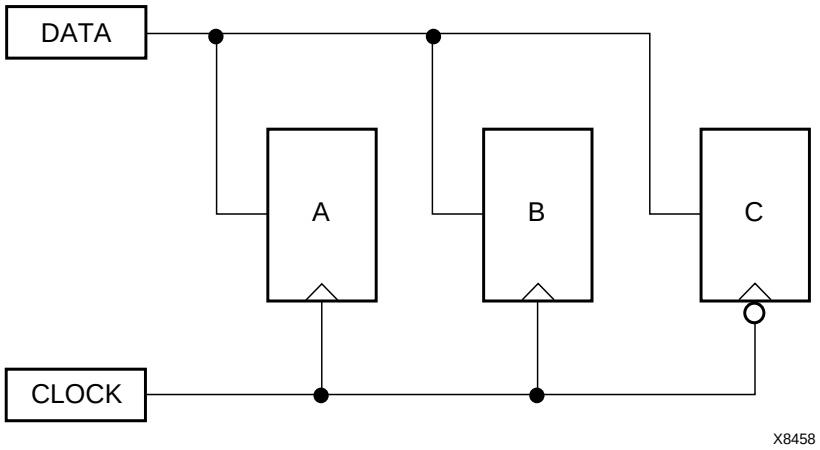


Figure 87-4: **Using Timegroups with Registers**

You can define time groups for the registers A, B and C, even though these registers have the same data and clock source. The syntax is as follows.

- UCF / PCF syntax

  ```
  TIMEGRP “B”=RISING FFS; TIMEGRP “C”=FALLING FFS;
  ```

- Schematic syntax attached to DATA

  ```
  OFFSET=IN 10 BEFORE “CLOCK” TIMEGRP “AB”
  OFFSET=IN 20 BEFORE “CLOCK” TIMEGRP “C”
  ```

- UCF syntax

  ```
  NET “DATA” OFFSET=IN 10 BEFORE “CLOCK” TIMEGRP “AB”;
  NET “DATA” OFFSET=IN 20 BEFORE “CLOCK” TIMEGRP “C”;
  ```

- PCF syntax

  ```
  COMP “DATA” OFFSET=IN 10 BEFORE COMP “CLOCK” TIMEGRP “AB”;
  COMP “DATA” OFFSET=IN 20 BEFORE COMP “CLOCK” TIMEGRP “C”;
  ```

Even though the registers A, B and C have a common data and clock source, timing analysis applies two different offsets (10 ns and 20 ns). Registers A and B belong to the offset with 10 ns, and Register C belongs to the offset with 20 ns.

However, you must use some caution when using timegroups with registers. Consider the following diagram.

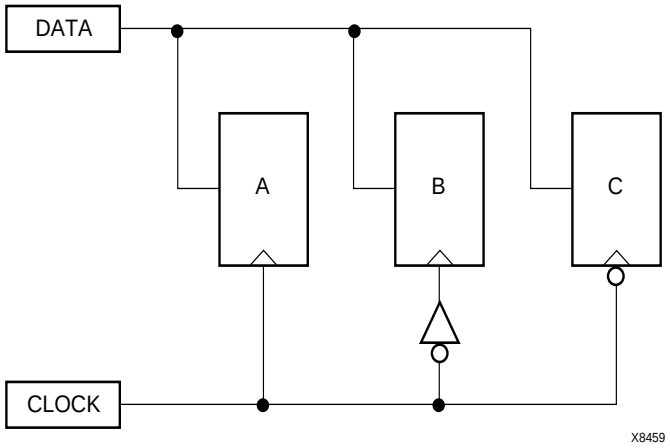


Figure 87-5: **Problematic Timegroup Definition**

This circuit is identical to Figure 87-4 except that an inverter has been inserted in the path to Register B. In this instance, even though this register is a member of the time group whose offset triggers on the rising edge, the addition of the inverter classifies register B as triggering on the falling edge like Register C.

Normally, the tools will move an inverter to the register, in which case, B would be a part of the timegroup “Falling”. However if the clock is gated with logic that inverts, then the inverter will not become part of the register. In that case, one way to solve this problem is to create a timegroup with an exception for Register B.

See “Creating Groups by Exclusion” for details.

OFFSET Examples

Schematic

Attach to a specific net.

Attribute Name—OFFSET

Attribute Values—IN | OUT *offset_time* BEFORE | AFTER *clk_pad_netname*

VHDL

Not applicable, use OFFSET_IN_BEFORE, OFFSET_OUT_AFTER.

Verilog

Not applicable, use OFFSET_IN_BEFORE, OFFSET_OUT_AFTER..

ABEL

Not applicable.

UCF/NCF

UCF syntax

```
TIMEGRP "name" OFFSET = {IN|OUT} offset_time [units] {BEFORE|AFTER}
"clk_name" [TIMEGRP "group_name"];
```

The following example specifies that the data will be present on input43 at least 20 ns before the triggering edge of the clock signal CLOCK.

```
NET "input43" OFFSET=IN 20 BEFORE "CLOCK";
```

XCF

Same as the UCF syntax.

Only OFFSET IN BEFORE and OFFSET OUT AFTER are supported. Two methods with some limitations are supported:

- Global method without TIMEGRP specification

  ```
  OFFSET = IN 3 ns BEFORE clk;
  OFFSET = OUT 3 ns AFTER clk;
  ```

- Net-specific method without TIMEGRP specification

  ```
  NET STRTSTOP OFFSET = IN 3 ns BEFORE clk;
  NET ONESOUT OFFSET = OUT 3 ns AFTER clk;
  ```

Alternate Method is not yet supported.

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

Set the OFFSET IN BEFORE constraint by setting Pad to Setup times in the Global, Ports, or Advanced tab.

Set the OFFSET OUT AFTER constraint by setting Clock to Pad times in the Global, Ports, or Advanced tabs.

PCF

See "OFFSET Syntax".

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

OFFSET -- Constraining Dual Data Rate (DDR) IOs

OFFSET OUT CONSTRAINTS -- DDR

The OFFSET OUT constraint is with respect to only a single edge of the input clock pad. Therefore, if you are using multiple clock phases (as is typically the case with source synchronous designs), the OFFSET OUT constraint must be manually adjusted by the clock phase.

Assume all outputs will be with respect to the rising edge of *clk_p* (this is specified as the HIGH keyword in the period constraint), and the clock to output budget allows for 6.0ns for the main data path. Therefore, the *tx_data* clocked by *clk0* should reach the pad 6.0ns after a rising edge at the clock input pad, *clk*_p. The design clocks out DDR data, which is driven by *clk0* and local inversion *(~clk*0). Therefore, the *tx_data* clocked by *~clk0* should reach the pad 6.0ns + ½ clock cycle after a rising edge at *clk*_p.

This source synchronous design requires that the forwarded clock *(tx_cl*k) be sent center-aligned with data *(tx_data*). Therefore, *tx_clk* is forwarded by *clk90* and *clk27*0. It is expected that the rising edge of *tx_clk* will reach the pad 6.0ns + ¼ clock cycle after a rising edge at *clk*_p. Likewise, the falling edge should occur 6.0ns + ¾ clock cycle after a rising edge at *clk*_p.

The Xilinx tools do not automatically adjust any of the clock phases for you. Therefore, they must be manually adjusted when creating the IO constraints.

In this sample design, there is additional test logic *(test_por*t) driven off the *clk0* domain. This logic is non-timing critical, and is not registered in the IOB (perhaps due to IO placement restrictions or some other reason). Therefore, the clock to output budget allows 10.0ns for these signals.

There are several ways that these output paths might be constrained, one example is listed below:

```
# Create main PERIOD constraint. This is required in order
# to pass the phase keyword to each of the derived clocks
# (clk0, clk90, clk270)
# Note that the HIGH keyword indicates all transitions are with respect
# to the rising clock edge of clk_p.

NET “clk_p” TNM_NET = “CLK”;
TIMESPEC “TS_CLK” = PERIOD “CLK” 8.0 ns HIGH 50%;

# Create separate timing groups based off each clock domain

NET “clk0” TNM = “CLK0_GRP_DDR” ;
NET “clk90” TNM = “CLK90_GRP” ;
NET “clk270” TNM = “CLK270_GRP” ;

# clk0 contains both rising and falling clock edges. Therefore
# break the clk0 group (CLK0_GRP_DDR) into two timing groups – required
# to constrain each group separately.

TIMEGRP “CLK0_GRP_ALL” = RISING “CLK0_GRP_DDR” ; # clk0 registers
TIMEGRP “CLK180_GRP” = FALLING “CLK0_GRP_DDR” ; # ~clk0 registers

# The new clk0 group (CLK0_GRP_ALL) contains both the tx_data ports that
# should be constrained, but also the test_port signals that are slower.
```

```
# Add these slower signals to their own group, and remove them from
# the main clk0 group.

INST “test_port” TNM = “TEST_GRP” ;
TIMEGRP “CLK0_GRP” = “CLK0_GRP_ALL” EXCEPT “TEST_GRP” ;

# Now that all groups are created, generate the OFFSET constraints.
# Recall that the OFFSET constraints must be manually adjusted to
# account for the clock phase. In this design, clock cycle = 8.0ns (as
# defined by the PERIOD).

OFFSET = OUT 6.0 ns AFTER “clk_p” TIMEGRP “CLK0_GRP” ; #6.0ns
OFFSET = OUT 8.0 ns AFTER “clk_p” TIMEGRP “CLK90_GRP” ;
#6.0ns + ¼ clock cycle

OFFSET = OUT 10.0 ns AFTER “clk_p” TIMEGRP “CLK180_GRP”;
#6.0ns + ½ clock cycle

OFFSET = OUT 12.0 ns AFTER “clk_p” TIMEGRP “CLK270_GRP”;
#6.0ns + ¾ clock cycle

OFFSET = OUT 10.0 ns AFTER “clk_p” TIMEGRP “TEST_GRP” ; #10.0ns
```

The resulting timing report should show the data path, the clock path, and also include the clock arrival time (clock phase). Looking at the timing report for clk0 and clk180 shows this:

```
================================================================================

Timing constraint: OFFSET = OUT 6 nS AFTER COMP "clk_p" TIMEGRP
"CLK0_GRP" ;

4 items analyzed, 0 timing errors detected.

Minimum allowable offset is 5.097ns.

--------------------------------------------------------------------------------

Slack: 0.903ns (requirement - (clock arrival + clock path + data path))
Source: clk_p (PAD)
Destination: tx_data<0> (PAD)
Source Clock: clk0 rising at 0.000ns
Requirement: 6.000ns
Data Path Delay: 5.667ns (Levels of Logic = 0)
Clock Path Delay: -0.570ns (Levels of Logic = 3)

================================================================================

Timing constraint: OFFSET = OUT 10 nS AFTER COMP "clk_p" TIMEGRP
"CLK180_GRP" ;

4 items analyzed, 0 timing errors detected.

Minimum allowable offset is 9.097ns.

--------------------------------------------------------------------------------

Slack: 0.903ns (requirement - (clock arrival + clock path + data path))
Source: clk_p (PAD)
Destination: tx_data<0> (PAD)
Source Clock: clk0 falling at 4.000ns
Requirement: 10.000ns
Data Path Delay: 5.667ns (Levels of Logic = 0)
Clock Path Delay: -0.570ns (Levels of Logic = 3)
```

As can be seen, the CLK0_GRP is clocked out at time 0ns by the clk0 clock. Likewise, the CLK180_GRP is clocked out at ½ clock cycle (8.0ns / 2 = 4.0ns) by the falling edge of clk0.

Similarly, the CLK90_GRP should be clocked out at ¼ clock cycle (8.0ns / 4 = 2.0ns) by clk90 clock. The CLK270_GRP should be clocked out at ¾ clock cycle (8.0ns * ¾ = 6.0ns) by clk270 clock.

```
================================================================================
Timing constraint: OFFSET = OUT 8 nS AFTER COMP "clk_p" TIMEGRP
"CLK90_GRP" ;
1 item analyzed, 0 timing errors detected.
Minimum allowable offset is 5.104ns.
--------------------------------------------------------------------------------
Slack: 2.896ns (requirement - (clock arrival + clock path + data path))
Source: clk_p (PAD)
Destination: tx_clk (PAD)
Source Clock: clk90 rising
Requirement: 8.000ns
Data Path Delay: 5.667ns (Levels of Logic = 0)
Clock Path Delay: -0.563ns (Levels of Logic = 3)
```

If you have items analyzed in the clk90 period, then the report would look as expected:

```
================================================================================
Timing constraint: OFFSET = OUT 8 nS AFTER COMP "clk_p" TIMEGRP
"CLK90_GRP" ;
1 item analyzed, 0 timing errors detected.
Minimum allowable offset is 5.104ns.
--------------------------------------------------------------------------------
Slack: 2.896ns (requirement - (clock arrival + clock path + data path))
Source: clk_p (PAD)
Destination: tx_clk (PAD)
Source Clock: clk90 rising at 2.000ns
Requirement: 8.000ns
Data Path Delay: 5.667ns (Levels of Logic = 0)
Clock Path Delay: -0.563ns (Levels of Logic = 3)
```

Finally, if the LOW keyword was specified in the period constraint:

```
NET “clk_p” TNM_NET = “CLK”;
TIMESPEC “TS_CLK” = PERIOD “CLK” 8.0 ns LOW 50%;
```

Then all output constraints would be with relation to the falling edge of *clk*_p. For the above example, all constraints would now be shifted – the clk180 constraint would now occur at time 0ns, clk270 at ¼ clock cycle, clk0 at ½ clock cycle, and clk90 at ¾ clock cycle.

```
================================================================================
Timing constraint: OFFSET = OUT 10 nS AFTER COMP "clk_p" TIMEGRP
"CLK0_GRP" ;
4 items analyzed, 0 timing errors detected.
Minimum allowable offset is 9.097ns.
--------------------------------------------------------------------------------
Slack: 0.903ns (requirement - (clock arrival + clock path + data path))
Source: clk_p (PAD)
Destination: tx_data<0> (PAD)
Source Clock: clk0 rising at 4.000ns
Requirement: 10.000ns
Data Path Delay: 5.667ns (Levels of Logic = 0)
Clock Path Delay: -0.570ns (Levels of Logic = 3)
================================================================================
Timing constraint: OFFSET = OUT 12 nS AFTER COMP "clk_p" TIMEGRP
"CLK90_GRP" ;
```

```
1 item analyzed, 0 timing errors detected.
Minimum allowable offset is 11.152ns.
--------------------------------------------------------------------------------
Slack: 0.848ns (requirement - (clock arrival + clock path + data path))
Source: clk_p (PAD)
Destination: tx_clk (PAD)
Source Clock: clk90 rising at 6.000ns
Requirement: 12.000ns
Data Path Delay: 5.667ns (Levels of Logic = 0)
Clock Path Delay: -0.515ns (Levels of Logic = 3)
================================================================================
Timing constraint: OFFSET = OUT 6 nS AFTER COMP "clk_p" TIMEGRP
"CLK180_GRP" ;
4 items analyzed, 0 timing errors detected.
Minimum allowable offset is 5.097ns.
--------------------------------------------------------------------------------
Slack: 0.903ns (requirement - (clock arrival + clock path + data path))
Source: clk_p (PAD)
Destination: tx_data<0> (PAD)
Source Clock: clk0 falling at 0.000ns
Requirement: 6.000ns
Data Path Delay: 5.667ns (Levels of Logic = 0)
Clock Path Delay: -0.570ns (Levels of Logic = 3)
================================================================================
Timing constraint: OFFSET = OUT 8 nS AFTER COMP "clk_p" TIMEGRP
"CLK270_GRP" ;
1 item analyzed, 0 timing errors detected.
Minimum allowable offset is 7.140ns.
--------------------------------------------------------------------------------
Slack: 0.860ns (requirement - (clock arrival + clock path + data path))
Source: clk_p (PAD)
Destination: tx_clk (PAD)
Source Clock: clk270 rising at 2.000ns
Requirement: 8.000ns
Data Path Delay: 5.667ns (Levels of Logic = 0)
Clock Path Delay: -0.527ns (Levels of Logic = 3)
```

OFFSET IN CONSTRAINTS

Similar to the OFFSET OUT constraint, the OFFSET IN constraint is with respect to either the rising or falling clock edge of the clock pad. Therefore, if you are using multiple clock phases, the OFFSET IN constraint must be manually adjusted by the clock phase.

As an example, assume the following circuit:

Assume all outputs will be with respect to the rising edge of *clk_p* (specified as the HIGH keyword in the period constraint), and the input setup budget is 2.0ns. Therefore, the data should be stable on *din* 2.0ns before the rising edge of *clk*_p. This input flop captures DDR data, and the falling edge data will likewise be valid 2.0ns before the falling edge of clk_p. Recall that the OFFSET constraint is only with respect to one clock edge (in this example the rising). The falling edge data will not be stable until ½ clock cycle after the rising edge of *clk*_p. Therefore, subtract ½ clock cycle from the OFFSET constraint.

There are several ways that these input paths may be constrained, one example is listed below:

```
# Create main PERIOD constraint.

NET clk_p TNM_NET = CLK;
TIMESPEC TS_CLK = PERIOD CLK 8.0 ns HIGH 50%;

# Create separate timing groups based off each clock domain

NET clk0 TNM = CLK0_GRP_DDR;
TIMEGRP CLK0_GRP = RISING CLK0_GRP_DDR ; # clk0 registers
TIMEGRP CLK180_GRP = FALLING CLK0_GRP_DDR ; # ~clk0 registers

# Now that all groups are created, generate the OFFSET constraints.
# Recall that the OFFSET constraints must be manually adjusted to
# account for the clock phase.

OFFSET = IN 2.0 ns BEFORE clk_p TIMEGRP CLK0_GRP ; # 2.0ns
OFFSET = IN -2.0 ns BEFORE clk_p TIMEGRP CLK180_GRP ;
# 2.0ns – ½ clock cycle
```

For the rising edge data, these constraints state that data will be valid 2.0ns before the rising edge of *clk*_p. Because the rising edge is defined in the period constraint, the falling edge data must also be with respect to this edge. Therefore, the falling edge data will not be valid until 2.0ns after the *clk*_p, which generates a negative offset before constraint.

```
================================================================================

Timing constraint: OFFSET = IN 2 nS BEFORE COMP "clk_p" TIMEGRP
"CLK0_GRP" ;

4 items analyzed, 0 timing errors detected.

Minimum allowable offset is 1.488ns.

--------------------------------------------------------------------------------

Slack: 0.512ns (requirement - (data path - clock path - clock arrival))
Source: din<0> (PAD)
Destination: doutp_d1_0 (FF)
Destination Clock: clk0 rising at 0.000ns
Requirement: 2.000ns
Data Path Delay: 0.918ns (Levels of Logic = 0)
Clock Path Delay: -0.570ns (Levels of Logic = 3)

================================================================================

Timing constraint: OFFSET = IN -2000 pS BEFORE COMP "clk_p" TIMEGRP
"CLK180_GRP" ;

4 items analyzed, 0 timing errors detected.

Offset is -2.512ns.

Negative offset in this situation may cause a hold violation.

--------------------------------------------------------------------------------

Slack: 0.512ns (requirement - (data path - clock path - clock arrival))
Source: din<0> (PAD)
Destination: doutn_d1_0 (FF)
Destination Clock: clk0 falling at 4.000ns
Requirement: -2.000ns
Data Path Delay: 0.918ns (Levels of Logic = 0)
Clock Path Delay: -0.570ns (Levels of Logic = 3)
```

The timing tools report that the negative offset may cause a hold violation. However, this warning was put in the tools to flag non-DDR designs where the user has a data path that is less than the clock path. In the DDR case, this does not hold true as can be seen from the

OFFSET IN constraint reports above – the data path is always longer than the clock path – and this warning can safely be ignored.

If the LOW keyword is given, the same rules will apply as existed for the OFFSET OUT case. The clk0 clock arrival time will now be rising at 4.0ns, and the clk180 falling time will be at 0ns.

Sample Verilog source code is given in "Verilog Source Code--DDR". This code combines the two previous figures into a simple test design. "UCF File -- DDR" contains the corresponding constraints (UCF) file

Verilog Source Code--DDR

```
‘define WIDTH 4
module test
(
 clk_p,
 din,
 rst,
 tx_data,
 tx_clk,
 test_port
);
input               clk_p;
input [‘WIDTH-1:0]  din;
input               rst;
output [‘WIDTH-1:0] tx_data;
output              tx_clk;
output              test_port;
reg                 test_port;
reg [‘WIDTH-1:0]    doutp;

reg [‘WIDTH-1:0]    doutn;
reg [‘WIDTH-1:0]    doutp_d1;
reg [‘WIDTH-1:0]    doutn_d1;

wire clk_ibuf;
wire clk0_unbuf;
wire clk90_unbuf;
wire clk270_unbuf;
wire clk0;
wire clk90;
wire clk180;
wire clk270;

IBUFG CLK_IBUF (.I(clk_p), .O(clk_ibuf));
DCM      DCM_A (.CLKIN (clk_ibuf),
                .CLKFB (clk0),
                .CLK0 (clk0_unbuf),
                .CLK90 (clk90_unbuf),
                .CLK180 (),
                .CLK270 (clk270_unbuf));
BUFG CLK0_BUF   (.I(clk0_unbuf), .O(clk0));
BUFG CLK90_BUF  (.I(clk90_unbuf), .O(clk90));
BUFG CLK270_BUF (.I(clk270_unbuf), .O(clk270));

assign clk180 = ~clk0;

always @(posedge clk0 or posedge rst)
```

```
begin
   if (rst)
       doutp_d1 <= 0;
   else
       doutp_d1 <= din;
end

always @(posedge clk0)
begin
   doutp <= doutp_d1;
end

always @(posedge clk180 or posedge rst)
begin
   if (rst)
       doutn_d1 <= 0;
   else
       doutn_d1 <= din;
end

always @(posedge clk180)
begin
   doutn <= doutn_d1;
end

always @(posedge clk0)
begin
   test_port <= doutp_d1[0] & doutn_d1[0];
end

FDDRRSE U0_DDR (
       .D0(doutp[0]),
       .D1(doutn[0]),
       .C0(clk0),
       .C1(clk180),
       .CE(1'b1),
       .R(1'b0),
       .S(1'b0),
       .Q(tx_data[0])
);

FDDRRSE U1_DDR (
       .D0(doutp[1]),
       .D1(doutn[1]),
       .C0(clk0),
       .C1(clk180),
       .CE(1'b1),
       .R(1'b0),
       .S(1'b0),
       .Q(tx_data[1])
);

FDDRRSE U2_DDR (
       .D0(doutp[2]),
       .D1(doutn[2]),
       .C0(clk0),
       .C1(clk180),
       .CE(1'b1),
       .R(1'b0),
```

```
        .S(1'b0),
        .Q(tx_data[2])
);

FDDRRSE U3_DDR (
        .D0(doutp[3]),
        .D1(doutn[3]),
        .C0(clk0),
        .C1(clk180),
        .CE(1'b1),
        .R(1'b0),
        .S(1'b0),
        .Q(tx_data[3])
);

FDDRRSE CLK_DDR (
        .D0(1'b1),
        .D1(1'b0),
        .C0(clk90),
        .C1(clk270),
        .CE(1'b1),
        .R(1'b0),
        .S(1'b0),
        .Q(tx_clk)
);

endmodule
```

UCF File -- DDR

```
# Create main PERIOD constraint. This is required in order
# to pass the phase keyword to each of the derived clocks
# (clk0, clk90, clk270)
# Note that the HIGH keyword indicates all transitions are with respect
# to the rising clock edge of clk_p.

NET "clk_p" TNM_NET = "CLK";
TIMESPEC "TS_CLK" = PERIOD "CLK" 8.0 ns HIGH 50%;

# Create separate timing groups based off each clock domain

NET "clk0" TNM = "CLK0_GRP_DDR" ;
NET "clk90" TNM = "CLK90_GRP" ;
NET "clk270" TNM = "CLK270_GRP" ;

# clk0 contains both rising and falling clock edges. Therefore
# break the clk0 group (CLK0_GRP_DDR) into two timing groups - required
# to constrain each group separately.

TIMEGRP "CLK0_GRP_ALL" = RISING "CLK0_GRP_DDR" ; # clk0 registers
TIMEGRP "CLK180_GRP" = FALLING "CLK0_GRP_DDR" ; # ~clk0 registers

# The new clk0 group (CLK0_GRP_ALL) contains both the tx_data ports that
# should be constrained, but also the test_port signals that are slower.
# Add these slower signals to their own group, and remove them from
# the main clk0 group.

INST "test_port" TNM = "TEST_GRP" ;
TIMEGRP "CLK0_GRP" = "CLK0_GRP_ALL" EXCEPT "TEST_GRP" ;

# Now that all groups are created, generate the OFFSET constraints.
# Recall that the OFFSET constraints must be manually adjusted to
# account for the clock phase. In this design, clock cycle = 8.0ns (
# as defined by the PERIOD).
```

```
OFFSET = OUT 6.0 ns AFTER "clk_p" TIMEGRP "CLK0_GRP" ; #6.0ns
OFFSET = OUT 8.0 ns AFTER "clk_p" TIMEGRP "CLK90_GRP" ;
#6.0ns + ¼ clock cycle

OFFSET = OUT 10.0 ns AFTER "clk_p" TIMEGRP "CLK180_GRP";
#6.0ns + ½ clock cycle

OFFSET = OUT 12.0 ns AFTER "clk_p" TIMEGRP "CLK270_GRP";
#6.0ns + ¾ clock cycle

OFFSET = OUT 10.0 ns AFTER "clk_p" TIMEGRP "TEST_GRP" ; #10.0ns
OFFSET = IN 2.0 ns BEFORE clk_p TIMEGRP CLK0_GRP ; # 2.0ns

OFFSET = IN -2.0 ns BEFORE clk_p TIMEGRP CLK180_GRP ;
# 2.0ns - ½ clock cycle
```

OFFSET -- Constraining DDR Registers and Negative-Edge-to-Negative-Edge Paths

When the timing tools are adding or subtracting half of the period to OFFSETs for DDR flip-flops and negative-edge-clocked output flip-flops, you need to know how to constrain these.

1. Group the negative groups separately, and then modify the constraint value to take the difference between clock edges into account.
2. Assuming that the PERIOD constraint specifies a High starting edge for the negative flip-flop groups, subtract half of the clock period from the OFFSET IN requirement and add half of the clock period to the OFFSET OUT requirement.

For example:

```
NET "main_clk" TNM_NET = "main_clk";

TIMESPEC "TS_main_clk" = PERIOD "main_clk" 16 ns HIGH 50%;

INST DDR_inputs* TNM = IN_DDR; #IN_DDR includes only pads
INST DDR_outputs* TNM = OUT_DDR; #OUT_DDR includes only pads

TIMEGRP "falling_reg" = FALLING "main_clk";
#falling _reg includes synchronous elements
```

or you can use the following code:

```
INST "IN_DDR_01" TNM = "falling_reg";
#falling_reg includes synchronous elements

TIMEGRP "IN_DDR" OFFSET = IN 10 ns BEFORE "main_clk";

TIMEGRP "IN_DDR" OFFSET = IN 2 ns BEFORE "main_clk" TIMEGRP
"falling_reg"; (User Manually Adjusts the Requirement)


TIMEGRP "OUT_DDR" OFFSET = OUT 12 ns AFTER "main_clk";

TIMEGRP "OUT_DDR" OFFSET = OUT 20 ns AFTER "main_clk" TIMEGRP
"falling_reg"; (User Manually Adjusts the Requirement)
```

For duty cycles other than 50-50 that are specified with a HIGH PERIOD TIMESPEC, take the difference from the rising edge to the falling edge and apply it to the negative edge group. For a PERIOD that is specified as a Low starting edge, apply the falling-edge-to-rising-edge time to the positive edge group.

ONESHOT

ONESHOT Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

ONESHOT Applicable Elements

- CAPTURE_SPARTAN2 for Spartan-II only
- CAPTURE_SPARTAN3 for Spartan-3 only
- CAPTURE_VIRTEX for Virtex
- CAPTURE_VIRTEX2 for Virtex-II, Virtex-II Pro, and Virtex-II Pro X
- CAPTURE_VIRTEX4

ONESHOT Description

ONESHOT is a basic readback constraint, related to readback timing. It limits the capture of registers for readback to a single capture of all register information. After a trigger (transition on CLK while CAP is asserted), all register information is captured and no

additional captures can occur until the readback operation is completed. Without ONESHOT, data is captured after every trigger.

ONESHOT Propagation Rules

It is illegal to attach ONESHOT to a signal or design element.

ONESHOT Syntax Examples

Schematic

Attach to a CAPTURE_*xx* instance.

Attribute Name—ONESHOT

Attribute Value—TRUE, FALSE

VHDL

Before using ONESHOT, declare it with the following syntax:

```
attribute oneshot: string;
```

After ONESHOT has been declared, specify the VHDL constraint as follows:

```
attribute oneshot of {component_name|label_name}: {component|label} is
“yes”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
 // synthesis attribute oneshot [of] {module_name|instance_name} [is]
“yes”;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

Not yet supported.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

OPEN_DRAIN

OPEN_DRAIN Architecture Support

The following table lists supported and unsupported architectures.:

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	No
Spartan-3E	No
Virtex-II	No
Virtex-II Pro	No
Virtex-II Pro X	No
Virtex-4	No
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	Yes

OPEN_DRAIN Applicable Elements

Output pads and pad nets.

OPEN_DRAIN Description

CoolRunner-II outputs can be configured to drive the primary macrocell output function as an open-drain output signal on the pin. The OPEN_DRAIN constraint applies to non 3-state (always active) outputs in the design. The output structure is configured as open-drain so that a one state on the output signal in the design produces a high-Z on the device pin instead of a driven High voltage. Note: The high-Z behavior associated with the OPEN_DRAIN constraint is not exhibited during functional simulation, but will be represented accurately during post-fit timing simulation. The logically-equivalent alternative to using the OPEN_DRAIN constraint is to take the original output-pad signal in the design and use it as a 3-state disable for a constant-zero output data value. The CPLD Fitter automatically optimizes all 3-state outputs with constant-zero data value in the design to take advantage of the open-drain capability of the device.

OPEN_DRAIN Propagation Rules

The constraint is a net or signal constraint. Any attachment to a macro, entity, or module is illegal.

OPEN_DRAIN Syntax Examples

Schematic

Attach to an output pad net.

Attribute Name—OPEN_DRAIN

Attribute Values—TRUE, FALSE

VHDL

Before using OPEN_DRAIN, declare it with the following syntax:

```
attribute OPEN_DRAIN: string;
```

After OPEN_DRAIN has been declared, specify the VHDL constraint as follows:

```
attribute OPEN_DRAIN of signal_name : signal is “TRUE”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute OPEN_DRAIN [of] signal_name [is] “TRUE”;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

```
XILINX PROPERTY 'OPEN_DRAIN mysignal';
```

UCF/NCF File

```
NET “mysignal” OPEN_DRAIN;
```

XCF

```
BEGIN MODEL “entity_name”
 NET  "signal_name" OPEN_DRAIN=true;
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

XST Command Line

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

Project Navigator

Not applicable.

OPT_EFFORT

OPT_EFFORT Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

OPT_EFFORT Applicable Elements

Any macro or hierarchy level.

OPT_EFFORT Description

OPT_EFFORT is a basic placement and routing constraint. It defines an effort level used by the optimizer.

OPT_EFFORT Propagation Rules

OPT_EFFORT is a macro, entity, module constraint. Any attachment to a net or signal is illegal.

OPT_EFFORT Syntax Examples

Schematic

Attach to a macro.

Attribute Name—OPT_EFFORT

Attribute Values—Default (Low), Lowest, Low, Normal, High, Highest

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

The following statement attaches a High effort of optimization to all of the logic contained within the module defined by instance $1I678/adder.

```
INST “$1I678/adder” OPT_EFFORT=HIGH;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Define globally with the Place and Route Effort Level (Overall) option in the Place and Route Properties tab of the Process Properties dialog box in the Project Navigator. The default is Low.

With a design selected in the Sources window, right-click Implement Design in the Processes window to access the appropriate Process Properties dialog box.

OPT_LEVEL

OPT_LEVEL Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

OPT_LEVEL Applicable Elements

OPT_LEVEL can be applied globally or to an entity or module.

OPT_LEVEL Description

OPT_LEVEL is a synthesis constraint. It defines the synthesis optimization effort level. Allowed values are **1** (normal optimization) and **2** (higher optimization). The default optimization effort level is **1** (Normal).

- 1 (Normal)

  Very fast processing, especially for hierarchical designs. This is the default mode and suggested for use with a majority number of designs.

- 2 (Higher Optimization)

  Time consuming processing—sometimes with better results in the number of macrocells or maximum frequency.

Note: In speed optimization mode, Xilinx strongly suggests using 1 (Normal) optimization effort for the majority of designs. Selecting optimization level 2 usually results in increased synthesis run times and does not always bring optimization gain.

OPT_LEVEL Propagation Rules

Applies to the entity or module to which it is attached.

OPT_LEVEL Syntax Examples

Schematic

Not applicable.

VHDL

Before using OPT_LEVEL, declare it with the following syntax:

```
attribute opt_level: string;
```

After OPT_LEVEL has been declared, specify the VHDL constraint as follows:

```
attribute opt_level of entity_name: entity is "{1|2}";
```

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
// synthesis attribute opt_level [of] module_name [is] "{1|2}";
```

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL "entity_name" opt_level={1|2};
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define OPT_LEVEL globally with the **-opt_level** command line option. Following is the basic syntax:

```
-opt_level {1|2}
```

The default is **1**.

Project Navigator

Define globally with the Optimization Effort option in the Synthesis Options tab of the Process Properties dialog box in the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

OPT_MODE

OPT_MODE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

OPT_MODE Applicable Elements

You can apply OPT_MODE globally or to an entity or module.

OPT_MODE Description

OPT_MODE is a synthesis constraint. It defines the synthesis optimization strategy. Available strategies are **speed** and **area**. By default, XST optimizations are speed-oriented.

- *speed*
  Priority is to reduce the number of logic levels and therefore to increase frequency.
- *area*
  Priority is to reduce the total amount of logic used for design implementation and therefore to improve design fitting.

OPT_MODE Propagation Rules

Applies to the entity or module to which it is attached.

OPT_MODE Syntax Examples

Schematic

Not applicable.

VHDL

Before using OPT_MODE, declare it with the following syntax:

```
attribute opt_mode: string;
```

After OPT_MODE has been declared, specify the VHDL constraint as follows:

```
attribute opt_mode of entity_name: entity is "{speed|area}";
```

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify OPT_MODE as follows:

```
// synthesis attribute opt_mode [of] module_name [is] {speed|area}
```

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL "entity_name" opt_mode={speed|area};
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-opt_mode** command line option of the **run** command. Following is the basic syntax:

```
-opt_mode {AREA|SPEED}
```

The default is **SPEED**.

Project Navigator

Define globally with the Optimization Goal option in the Synthesis Options tab of the Process Properties dialog box in the Project Navigator. The default is **Speed**.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

OPTIMIZE

OPTIMIZE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

OPTIMIZE Applicable Elements

Any macro, entity, module or hierarchy level.

OPTIMIZE Description

OPTIMIZE is a basic mapping constraint. It defines whether optimization is performed on the flagged hierarchical tree. OPTIMIZE has no effect on any symbol that contains no combinatorial logic, such as an input or output buffer.

OPTIMIZE Propagation Rules

Applies to the macro, entity, or module to which it is attached.

OPTIMIZE Syntax Examples

Schematic

Attach to a design element.

Attribute Name—OPTIMIZE

Attribute Values—AREA, SPEED, BALANCE, OFF

VHDL

Before using OPTIMIZE, declare it with the following syntax:

```
attribute optimize string;
```

After OPTIMIZE has been declared, specify the VHDL constraint as follows:

```
attribute optimize of {entity_name:entity} is
"{area|speed|balance|off}"
```

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify OPTIMIZE as follows:

```
 // synthesis attribute optimize [of] module_name [is]
{area|speed|balance|off}
```

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

The following statement specifies that no optimization be performed on an instantiation of the macro CTR_MACRO.

```
INST "/$1I678/CTR_MACRO" OPTIMIZE=OFF;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Define globally with the Optimization Strategy (Cover Mode) option in the Map Properties tab of the Process Properties dialog box in the Project Navigator. The default is Area.

With a design selected in the Sources window, right-click Implement Design in the Processes window to access the appropriate Process Properties dialog box.

OPTIMIZE_PRIMITIVES

OPTIMIZE_PRIMITIVES Architecture Support

The following table lists supported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

OPTIMIZE_PRIMITIVES Applicable Elements

Hierarchical blocks, components, and instances.

OPTIMIZE_PRIMITIVES Description

OPTIMIZE_PRIMITIVES is a synthesis constraint. Values are YES and NO (default). This constraint allows XST to optimize Xilinx library primitives that have been instantiated in HDL. By default, all instantiated primitives will be untouched and passed directly to the output netlist.

OPTIMIZE_PRIMITIVES Propagation Rules

Applies to the component or instance to which it is attached.

OPTIMIZE_PRIMITIVES Syntax Examples

Schematic

Attach to a valid instance.

Attribute Name—OPTIMIZE_PRIMITIVES

Attribute Value—YES and NO (Default)

VHDL

Before using OPTIMIZE_PRIMITIVES, declare it with the following syntax:

```
attribute OPTIMIZE_PRIMITIVES: string;
```

After OPTIMIZE_PRIMITIVES has been declared, specify the VHDL constraint as follows:

```
attribute OPTIMIZE_PRIMITIVES of
{component_name|entity_name|label_name}: {component|entity|label} is
"{yes|no}";
```

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute OPTIMIZE_PRIMITIVES [of]
{module_name|instance_name|signal_name} [is] {yes|no};
```

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name" OPTIMIZE_PRIMITIVES={yes|no};
```

XCF

```
MODEL "entity_name" OPTIMIZE_PRIMITIVES = {yes|no};
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Set globally with the Optimize Instantiated Primitives property in the Xilinx Specific Options tab of the Process Properties dialog box within the Project Navigator. With a source file selected in the Sources in Project window, right-click Synthesize in the Processes for Source window to access the appropriate Process Properties dialog box.

PARALLEL_CASE

PARALLEL_CASE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

PARALLEL_CASE Applicable Elements

You can apply PARALLEL_CASE to case statements in Verilog meta comments only.

PARALLEL_CASE Description

PARALLEL_CASE is an XST synthesis constraint.

PARALLEL_CASE Propagation Rules

Not applicable.

PARALLEL_CASE Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

The directive is exclusively available as a meta comment in your Verilog code and cannot be specified in a VHDL description or in a separate constraint file. The syntax differs from the standard meta comment syntax as shown in the following:

```
// synthesis parallel_case
```

Since the directive does not contain a target reference, the meta comment immediately follows the selector.

Example:

```
casex select // synthesis parallel_case
4'b1xxx: res = data1;
4'bx1xx: res = data2;
4'bxx1x: res = data3;
4'bxxx1: res = data4;
```

endcase

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define PARALLEL_CASE globally with the **-vlgcase** command line option of the **run** command. Following is the basic syntax:

```
-vlgcase {full|parallel|full-parallel}
```

Project Navigator

Not applicable.

PERIOD

PERIOD Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

Note: For XST, PERIOD applies to FPGAs only.

PERIOD Applicable Elements

Nets that feed forward to drive flip-flop clock pins

PERIOD Description

PERIOD is a basic timing constraint and synthesis constraint. A clock period specification checks timing between all synchronous elements within the clock domain as defined in the destination element group. The group may contain paths that pass between clock domains if the clocks are defined as a function of one or the other.

The period specification is attached to the clock net. The definition of a clock period is unlike a FROM-TO style specification because the timing analysis tools automatically take into account any inversions of the clock net at register clock pins, lock phase, and includes all synchronous item types in the analysis. It also checks for hold violations.

A PERIOD constraint on the clock net in the following figure would generate a check for delays on all paths that terminate at a pin that has a setup or hold timing constraint relative to the clock net. This could include the data paths CLB1.Q to CLB2.D, as well as the path EN to CLB2.EC (if the enable were synchronous with respect to the clock).

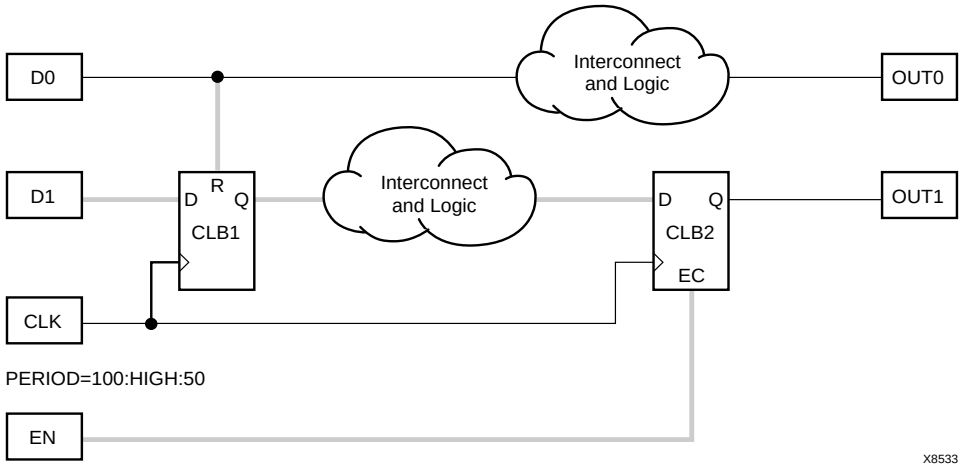


Figure 96-1: **Paths for PERIOD Constraint**

The timing tools do not check pad-to-register paths relative to setup requirements. For example, in the preceding figure, the path from D1 to Pin D of CLB1 is not included in the PERIOD constraint. The same is true for CLOCK_TO_OUT.

Special rules apply when using TNM and TNM_NET with the PERIOD constraint for DLLs and DCMs. These rules are explained in "PERIOD Specifications on CLKDLLs and DCMs".

Preferred Method

The preferred method for defining a clock period allows more complex derivative relationships to be defined as well as a simple clock period. The following constraint is defined using the TIMESPEC keyword in conjunction with a TNM constraint attached to the relevant clock net.

UCF Syntax

```
TIMESPEC "TSidentifier"=PERIOD "TNM_reference" period {HIGH | LOW}
[high_or_low_time]INPUT_JITTER;
```

where

- *identifier* is a reference identifier that has a unique name
- *TNM_reference* identifies the group of elements to which the period constraint applies. This is typically the name of a TNM_NET that was attached to a clock net, but it can be any TNM group or user group (TIMEGRP) that contains only synchronous elements.

The following rules apply:

- The variable name *period* is the required clock period.
- The default units for *period* are nanoseconds, but the number can be followed by ps, ns, us, or ms. The *period* can also be specified as a frequency value, using units of MHz, GHz, or kHZ.
- Units may be entered with or without a leading space.
- Units are case-insensitive.
- The **HIGH**|**LOW** keyword indicates whether the first pulse in the period is high or low, and the optional *high_or_low_time* is the polarity of the first pulse. This defines the initial clock edge and is used in the OFFSET constraint.
- If an actual time is specified, it must be less than the period.
- If no *high_or_low_time* is specified the default duty cycle is 50%.
- The default units for *high_or_low_time* is *ns*, but the number can be followed by *%* or by *ps, ns, us, or ms* to specify an actual time measurement.
- INPUT_JITTER is the random, peak-to-peak jitter on an input clock. The default units are picoseconds.

Examples

Clock net sys_clk has the constraint `tnm=master_clk` attached to it and the following constraint is attached to TIMESPEC.

UCF Syntax

```
TIMESPEC "TS_master"=PERIOD "master_clk" 50 HIGH 30;INPUT_JITTER 50
```

This period constraint applies to the net master_clk, and defines a clock period of 50 nanoseconds, with an initial 30 nanosecond high time, and INPUT_JITTER at 50 ps.

Another Method

Another method of defining a clock period is to attach the following constraint directly to a net in the path that drives the register clock pins.

Schematic Syntax

```
PERIOD = period {HIGH|LOW} [high_or_low_time] INPUT_JITTER
```

UCF Syntax

```
NET "net_name" PERIOD = period {HIGH|LOW} [high_or_low_time]
INPUT_JITTER;
```

The following rules apply:

- *period* is the required clock period. The default units are nanoseconds, but the timing number can be followed by ps, ns, us, or ms. The *period* can also be specified as a frequency value, using units of MHz, GHz, or kHZ.
- Units may be entered with or without a leading space.
- Units are case-insensitive.
- The **HIGH**|**LOW** keyword indicates whether the first pulse in the period is high or low, and the optional *high_or_low_time* is the duty cycle of the first pulse.
- If an actual time is specified, it must be less than the period.
- If no high or low time is specified the default duty cycle is 50%.

- The default unit for *high_or_low_time* is *ns*, but the number can be followed by *%* or by *ps*, *ns*, *us* or *ms* to specify an actual time measurement.

The PERIOD constraint is forward traced in exactly the same way a TNM would be and attaches itself to all of the synchronous elements that the forward tracing reaches. If a more complex form of tracing behavior is required (for example, where gated clocks are used in the design), you must place the PERIOD on a particular net or use the preferred method described in the next section.

Specifying Derived Clocks

The preferred method of defining a clock period uses an identifier, allowing another clock period specification to reference it. To define the relationship in the case of a derived clock, use the following syntax:

UCF Syntax

```
TIMESPEC "TSidentifier"=PERIOD "timegroup_name" "TSidentifier" [* or /]
factor PHASE [+ |-] phase_value [units];
```

where

- *identifier* is a reference identifier that has a unique name
- *factor* is a floating point number. You can omit the [* or /] factor if the specification being defined has the same value as the one being referenced (that is, they differ only in phase); this is the same as using "* 1".
- *phase_value* is a floating point number.
- *units* are ps, ms, us, or ns. The default is ns.

The following rules apply:

- If an actual time is specified it must be less than the period.
- If no *high_or_low_time* is specified, the default duty cycle is 50%.
- The default units for *high_or_low_time* is *ns*, but the number can be followed by *%* or by *ps*, *ns*, *us*, *or ms* to specify an actual time measurement.

Examples of a Primary Clock with Derived Clocks

Period for primary clock:

```
TIMESPEC “TS01” = PERIOD "clk0" 10.0 ns;
```

Period for clock phase-shifted forward by 180 degrees:

```
TIMESPEC “TS02” = PERIOD "clk180" TS01 PHASE + 5.0 ns;
```

Period for clock phase-shifted backward by 90 degrees:

```
TIMESPEC “TS03” = PERIOD "clk90" TS01 PHASE - 2.5 ns;
```

Period for clock doubled and phase-shifted forward by 180 degrees (which is 90 degrees relative to TS01):

```
TIMESPEC “TS04” = PERIOD "clk180" TS01 / 2 PHASE + 2.5 nS;
```

PERIOD Specifications on CLKDLLs and DCMs

When a TNM or TNM_NET property traces into an input pin on a DLL or DCM, it will be handled as described in the following paragraphs.

The checking and transformations described are performed by the logical TimeSpec processing code, which is run during NGDBuild, or the translate process. (The checking timing specifications status message indicates that the logical TimeSpec processing is being run.) The modifications are saved in the built NGD, used by the Mapper and the Map phase passed through the PCF file to the place and route (PAR) phase and TRACE.

However, note that the data saved in the built NGD is distinct from the original TimeSpec user-applied properties, which are left unchanged by this process. Therefore, the Constraints Editor will not see these new groups or specifications, but will see (and possibly modify) the original user-applied ones.

- Conditions for transformation

  When a TNM_NET property is traced into the CLKIN pin of a DLL or DCM, the TNM group and its usage are examined. The TNM will be pushed through the CLKDLL or DCM (as described below) only if the following conditions are met:

  - The TNM group is used in exactly *one* PERIOD specification.
  - The TNM group is *not* used in any FROM-TO or OFFSET specifications.
  - The TNM group is *not* referenced in any user group definition.

  If any of the above conditions are not met, the TNM will not be pushed through the CLKDLL / DCM, and a warning message will be issued. This will not prevent the TNM from tracing into other elements in the standard fashion, but if it traces nowhere else, and is used in a specification, an error will result.

- Definition of new PERIOD specifications

  If the CLK0 output on the CLKDLL or DCM is the only one being used (and neither CLKIN_DIVIDE_BY_2 nor CLKOUT_PHASE_SHIFT=FIXED are used), the original PERIOD specification will be simply transferred to that clock output.

  Otherwise, for each clock output pin used on the CLKDLL or DCM, a new TNM group will be created on the connected net, and a new PERIOD specification will be created for that group. The following table shows how the new PERIOD specifications will be defined, assuming an original PERIOD specification named TS_CLKIN:

Output Pin	New PERIOD Specification		
	Period Value	Phase Shift	Duty Cycle
CLK0	TS_CLKIN * 1	none	Copied from TS_CLKIN if DUTY_CYCLE_ CORRECTION is FALSE. Otherwise, 50%.
CLK90		PHASE + (*clk0_period* * 1 / 4)	
CLK180		PHASE + (*clk0_period* * 1 / 2)	
CLK270		PHASE + (*clk0_period* * 3 / 4)	
CLK2X	TS_CLKIN / 2	none	50%
CLK2X180		PHASE + (*clk2X_period* * 1 / 2)	

Output Pin	New PERIOD Specification		
	Period Value	Phase Shift	Duty Cycle
CLKDV	TS_CLKIN * *clkdv_divide* where *clkdv_divide* is the value of the CLKDV_DIVIDE property (default 2.0)	none	50% except for non-integer divides in high-frequency mode (CLKDLLHF, or DCM with DLL_FREQUENCY_MODE=HIGH): CLKDV_DIVIDE 1.5 33.33% HIGH 2.5 40.00% HIGH 3.5 42.86% HIGH 4.5 44.44% HIGH 5.5 45.45% HIGH 6.5 46.15% HIGH 7.5 46.67% HIGH
CLKFX	TS_CLKIN / *clkfx_factor* where *clkfx_factor* is the value of the CLKFX_MULTIPLY property (default 4.0) divided by the value of the CLKFX_DIVIDE property (default 1.0).	none	
CLKFX180		PHASE + (*clkfx_period* * 1 / 2)	50%

Note: The Period Value shown in this table assumes that the original specification, TS_CLKIN, is expressed as a time. If TS_CLKIN is expressed as a frequency, the multiply or divide operation will be reversed.

- If the DCM attribute FIXED_PHASE_SHIFT or VARIABLE_PHASE_SHIFT is used, the amount of phase specified is also included in the PHASE value.

PERIOD Propagation Rules

Applies to the signal to which it is attached.

PERIOD Syntax Examples

The following examples are for the “simple method.”

Schematic

Attach to a net. Following is an example of the syntax format.

Attribute Name—PERIOD

Attribute Values—*period* [*units*] [{**HIGH**|**LOW**} [*high_or_low_time*[*hi_lo_units*]]

VHDL

For XST, PERIOD only applies to a specific clock signal.

Before using PERIOD, declare it with the following syntax:

```
attribute period: string;
```

After PERIOD has been declared, specify the VHDL constraint as follows:

```
attribute period of signal_name : signal is "period [units]";
```

- *period* is the required clock period
- *units* is an optional field to indicate the units for a clock period. The default is nanoseconds (ns), but the timing number can be followed by ps, ns, or us to indicate the intended units.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

For XST, PERIOD only applies to a specific clock signal.

Specify as follows:

```
// synthesis attribute period [of] signal_name [is] "period [units]";
```

- *period* is the required clock period
- *units* is an optional field to indicate the units for a clock period. The default is nanoseconds (ns), but the timing number can be followed by ps, ns, or us to indicate the intended units.

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

TIMESPEC PERIOD Method (Primary Method)

UCF syntax:

```
TIMESPEC "TSidentifier"=PERIOD "TNM_reference period" [units] [{HIGH |
LOW} [high_or_low_time [hi_lo_units]]]INPUT_JITTER value [units]
;where
```

- *identifier* is a reference identifier that has a unique name
- *TNM_reference* is the identifier name that is attached to a clock net (or a net in the clock path) using the TNM or TNM_NET constraint.

When a TNM_NET constraint is traced into the CLKIN input of a DLL or DCM component, new PERIOD specifications may be created at the DLL / DCM outputs. If new PERIOD specifications are created, new TNM_NET groups to use in those specifications are also created.

Each new TNM_NET group is named the same as the corresponding DLL / DCM output net (*outputnetname*). The new PERIOD specification becomes "TS_*outputnetname*=PERIOD *outputnetname value units*."

The new TNM_NET groups are then traced forward from the DLL / DCM output net to tag all synchronous elements controlled by that clock signal. The new groups and specifications are shown in the timing analysis reports.

Rules

The following rules apply:

- *period* is the required clock period.
- *units* is an optional field to indicate the units for a clock period. The default is nanoseconds (ns), but the timing number can be followed by ps, ms, us, or % to indicate the intended units.
- HIGH or LOW indicates whether the first pulse is to be High or Low.
- *high_or_low_time* is the optional High or Low time, depending on the preceding keyword. If an actual time is specified, it must be less than the period. If no *high_or_low_time* is specified, the default duty cycle is 50 percent.
- *hi_lo_units* is an optional field to indicate the units for the duty cycle. The default is nanoseconds (ns), but the *high_or_low_time* number can be followed by ps, us, ms, or % if the High or Low time is an actual time measurement.

The following statement assigns a clock period of 40 ns to the net named CLOCK, with the first pulse being High and having a duration of 25 nanoseconds.

```
NET “CLOCK” PERIOD=40 HIGH 25;
```

NET PERIOD Method (Secondary Method)

```
NET “net_name” PERIOD=period [units] [{HIGH|LOW}
[high_or_low_time[hi_lo_units]]];
```

where

- *period* is the required clock period
- *units* is an optional field to indicate the units for a clock period. The default is nanoseconds (ns), but the timing number can be followed by ps, ns, or us to indicate the intended units.
- HIGH or LOW can be optionally specified to indicate whether the first pulse is to be High or Low.
- *hi_lo_units* can be ns, ps, or us. The default is ns.

The following rules apply:

- *high_or_low_time* is the optional High or Low time, depending on the preceding keyword.
- If an actual time is specified, it must be less than the period.
- If no *high_or_low_time* is specified, the default duty cycle is 50 percent.
- *hi_lo_units* is an optional field to indicate the units for the duty cycle.
- The default is nanoseconds (ns), but the *high_or_low_time* number can be followed by ps, us, ms, or % if the High or Low time is an actual time measurement.

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

In the Global tab grid, double-click the Period column in the row with the desired clock name and fill out the PERIOD dialog box.

XCF

Same as the UCF syntax.

Both the simple and preferred are supported with the following limitation: HIGH / LOW values are not taken into account during timing estimation / optimization and only propagated to the final netlist if WRITE_TIMING_CONSTRAINTS = yes.

PCF

"TS*identifier***"=PERIOD** *perioditem periodvalue*; INPUT_JITTER *value*

perioditem can be:

- NET *name*
- TIMEGRP *name*

periodvalue can be:

- TS*identifier* PHASE [+ | -] *time*
- TS*identifier* PHASE *time*
- TS*identifier* PHASE [+ | -] *time* [LOW | HIGH] *time*
- TS*identifier* PHASE *time* [LOW | HIGH] *time*
- TS*identifier* PHASE [+ | -] *time* [LOW | HIGH] *percent*
- TS*identifier* PHASE *time* [LOW | HIGH] *percent*

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

To set constraints, in the FPGA Editor main window, click Properties of Selected Items from the Edit menu. To set PERIOD constraint, click Properties of Selected Items from the Edit menu with a net selected. You can set the constraint from the Physical Constraints tab.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

PHASE_SHIFT

PHASE_SHIFT Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

PHASE_SHIFT Applicable Elements

DCM

PHASE_SHIFT Description

PHASE_SHIFT is an advanced DLL/DCM constraint. It adjusts the rising-edge skew between CLKIN and CLKFB at configuration when the CLKOUT_PHASE_SHIFT constraint is set to FIXED or VARIABLE mode. The phase shift value is specified as a fraction of the clock period as expressed in the following equations.

```
CLKIN_CLKFB_skew = (PHASE_SHIFT / 256) * CLKIN_PERIOD
PHASE_SHIFT = (256 x CLKIN_CLKFB_skew) / CLKIN_PERIOD
```

When the CLKOUT_PHASE_SHIFT constraint is set to FIXED, the value is static.

When the CLKOUT_PHASE_SHIFT constraint is set to VARIABLE, the skew can be dynamically adjusted after the DCM's LOCKED output goes High. The adjustments are

made using the PS* inputs/output of the DCM. Each time the PSEN input is activated for one period of PSCLK, the PHASE_SHIFT value is changed one unit. The PHASE_SHIFT value is increased one unit when PSINCDEC is High and decreased by one unit when PSINCDEC is Low. After an increment or decrement is completed, PSDONE goes High for a single PSCLK cycle to indicate that the adjustment is complete and the next change can be made. If the DCM is reset (RST goes High), the PHASE_SHIFT value reverts to the initial configured value.

PHASE_SHIFT Propagation Rules

It is illegal to attach PHASE_SHIFT to a net.

When attached to a design DCM, PHASE_SHIFT is propagated to all applicable elements of the DCM.

PHASE_SHIFT Syntax Examples

Schematic

Attach to a DCM instance.

Attribute Name—PHASE_SHIFT

Attribute Values—*n*

where *n* is a signed integer in the range -255 to +255.

VHDL

Before using PHASE_SHIFT, declare it with the following syntax:

```
attribute phase_shift: integer;
```

After PHASE_SHIFT has been declared, specify the VHDL constraint as follows:

```
attribute phase_shift of {component_name|label_name}:
{component|label} is "n";
```

where *n* is a signed integer in the range -255 to +255.

The default is 0 (zero).

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute phase_shift [of] {module_name|instance_name}
[is] n;
```

where *n* is a signed integer in the range -255 to +255.

The default is 0 (zero).

For a detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name" PHASE_SHIFT=n;
```

where *n* is a signed integer in the range -255 to +255.

The default is 0 (zero).

There are limits for the maximum skew that may be programmed in FIXED mode and VARIABLE mode. Therefore, the PHASE_SHIFT magnitude (absolute value) must also comply with the range limit specified in the following equation.

$$PHASE\_SHIFT_{MAG} \pounds (256 * maximum\_allowable\_skew) / PERIOD_{CLKIN}$$

See *The Programmable Logic Data Book* for the maximum skew values for FIXED and VARIABLE mode.

The following rules apply:

- If the initial PHASE_SHIFT value is out of range, the DCM will not lock.
- If the specified range limits are exceeded as adjustments occur during operation (CLKOUT_PHASE_SHIFT=VARIABLE), bit 0 of the STATUS output (the Phase Shift Overflow bit) goes True but LOCKED also remains True.

The following statement specifies a phase shift of 4.

```
INST "foo/bar" PHASE_SHIFT=+4;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Select a DCM component from the List window. Click editblock from the User toolbar that is located to the right of the List window. Click the F= button to display the PHASE_SHIFT in the lower portion of the Block window.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

PIN

PIN Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

PIN Applicable Elements

Nets.

PIN Description

The PIN constraint in conjunction with LOC defines a net location.

The PIN / LOC UCF constraint has the following syntax:

```
PIN "module.pin" LOC="location";
```

This UCF constraint is used in creating design flows. This UCF constraint is translated into a COMP / LOCATE constraint in the PCF file. This constraint has the following syntax in the PCF file:

```
COMP "name" LOCATE = SITE "location";
```

This constraint specifies that the pseudo component that will be created for the pin on the module should be located in the site location. Pseudo logic is only created when a net connects from a pin on one module to a pin on another module.

PIN Propagation Rules

Not applicable.

PIN Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF

```
PIN "module.pin" LOC=location;
```

NCF

Not applicable.

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

PRIORITY

PRIORITY Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

PRIORITY Applicable Elements

TIMESPECs.

PRIORITY Description

PRIORITY is an advanced timing constraint keyword. There may be situations where there is a conflict between two timing constraints that cover the same path. The lower the PRIORITY value, the higher the priority. This value does not affect which paths will be place and routed first. It only affects which constraint will control the path when two constraints of equal priority cover the same path.

The PRIORITY keyword cannot be used with the MAXDELAY or MAXSKEW constraint.

PRIORITY Propagation Rules

Not applicable.

PRIORITY Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

Defines the priority of a timing constraint using the following syntax.

```
normal_timespec_syntax PRIORITY integer;
```

where

- *normal_timespec_syntax* is a legal timing specification
- *integer* represents the priority (the smaller the number, the higher the priority)

The number can be positive, negative, or zero, and the value only has meaning when compared with other PRIORITY values. The lower the value, the higher the priority.

```
TIMESPEC "TS01"=FROM "GROUPA" TO "GROUPB" 40 PRIORITY 4;
```

XCF

Not yet supported.

Constraints Editor

Not applicable.

PCF

The same as UCF.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

PRIORITY_EXTRACT

PRIORITY_EXTRACT Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

PRIORITY_EXTRACT Applicable Elements

You can apply PRIORITY_EXTRACT globally or to an entity, module, or signal.

PRIORITY_EXTRACT Description

PRIORITY_EXTRACT is a synthesis constraint. It enables or disables priority encoder macro inference. Allowed values are **YES**, **NO** and **FORCE**. (**TRUE** and **FALSE** ones are available in XCF as well).

By default, priority encoder inference is enabled (**YES**). For each identified priority encoder description, based on some internal decision rules, XST will actually create a macro or optimize it with the rest of the logic. The **FORCE** value allows to override those decision rules and force XST to extract the macro.

Priority encoder rules are currently very restrictive. Based on architectural considerations, the **FORCE** value will allow you to override these rules and potentially improve the quality of your results.

PRIORITY_EXTRACT Propagation Rules

Applies to the entity, module, or signal to which it is attached.

PRIORITY_EXTRACT Syntax Examples

Schematic

Not applicable.

VHDL

Before using PRIORITY_EXTRACT, declare it with the following syntax:

```
attribute priority_extract: string;
```

After PRIORITY_EXTRACT has been declared, specify the VHDL constraint as follows:

```
attribute priority_extract of {signal_name|entity_name}:
{signal|entity} is "{yes|no|force}";
```

The default value is **YES.**

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
// synthesis attribute priority_extract [of] {module_name|signal_name}
[is] {yes|no|force};
```

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL "entity_name" priority_extract={yes|no|force|true|false};

BEGIN MODEL "entity_name"
 NET "signal_name"  priority_extract={yes|no|force|true|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-priority_extract** command line option of the **run** command. Following is the basic syntax:

```
-priority_extract {YES|NO|FORCE}
```

The default is **YES**.

Project Navigator

Set globally with the Priority Encoder Extraction option in the HDL Options tab of the Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

PROHIBIT

PROHIBIT Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

PROHIBIT Applicable Elements

Sites

PROHIBIT Description

PROHIBIT is a basic placement constraint and a modular design constraint. It disallows the use of a site within PAR, FPGA Editor, and the CPLD fitter.

Location Types for FPGAs

For an FPGA, use the following location types to define the physical location of an element.

Element Types	Location Specification	Meaning
IOBs		

	P12	IOB location (chip carrier)
	A12	IOB location (pin grid)
	T, B, L, R	Applies to IOBs and indicates edge locations (bottom, left, top, right) for Spartan-II, Spartan-IIE, Spartan-3, Virtex, Virtex-E, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4.
	LB, RB, LT, RT, BR, TR, BL, TL	Applies to IOBs and indicates half edges (left bottom, right bottom, and so forth) for Spartan-II, Spartan-IIE, Spartan-3, Virtex, Virtex-E, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4.
	Bank 0, Bank 1, Bank 2, Bank 3, Bank 4, Bank 5, Bank 6, Bank 7	Applies to IOBs and indicates half edges (banks) for Spartan-II, Spartan-IIE, Spartan-3, Virtex, Virtex-E, Virtex-II, Virtex-II Pro, Virtex-II Pro X, andVirtex-4.
CLBs		
	CLB_R4C3 (or .S0 or .S1)	CLB location for Spartan-II, Spartan-IIE, Virtex, and Virtex-E
	CLB_R6C8.S0 (or .S1)	Function generator or register slice for Spartan-II, Spartan-IIE, Virtex, and Virtex-E
Slices		
	SLICE_X22Y3	Slice location for Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4
TBUFs		
	TBUF_R6C7 (or .0 or .1)	TBUF location for Spartan-II, Spartan-IIE, Virtex, and Virtex-E
	TBUF_X6Y7	TBUF location for Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4
Block RAMs		
	RAMB4_R3C1	Block RAM location for Spartan-II, Spartan-IIE, Virtex, and Virtex-E
	RAMB16_X2Y56	Block RAM location for Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4
Multipliers		

	MULT18X18_X55Y82	Multiplier location for Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4
Global Clocks		
	GCLKBUF0 (or 1, 2, or 3)	Global clock buffer location for Spartan-II, Spartan-IIE, Virtex, and Virtex-E
	GCLKPAD0 (or 1, 2, or 3)	Global clock pad location for Spartan-II, Spartan-IIE, Virtex, and Virtex-E
Delay Locked Loops		
	DLL0 (or 1, 2, or 3)	Delay Locked Loop element location for Spartan-II, Spartan-IIE, Virtex, and Virtex-E
Digital Clock Manager:		
	DCM_X[A]Y[B]	Digital Clock Manager for Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4

You can use the wildcard character (*) to replace a single location with a range as shown in the following examples.

CLB_R*C5	Any CLB in column 5 of a Spartan-II, Spartan-IIE, Virtex, and Virtex-E
SLICE_X*Y5	Any slice of a Spartan-3, Virtex-II, Virtex-II Pro, Virtex-4, or Virtex-II Pro X device whose Y-coordinate is 5

The following are *not* supported:

- Dot extensions on ranges. For example, LOC=CLB_R0C0:CLB_R5C5.G.
- The wildcard character for Spartan-II, Spartan-IIE, Spartan-3, Virtex, Virtex-E, Virtex-II, Virtex-II Pro, and Virtex-II Pro X global buffer or DLL locations.

Location Types for CPLDs

CPLDs support only the location type *pin_name*, where *pin_name* is P*nn* for numeric pin names or *rc* for row-column pin names.

PROHIBIT Propagation Rules

It is illegal to attach PROHIBIT to a net, signal, entity, module, or macro.

PROHIBIT Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

In a UCF file, PROHIBIT must be preceded by the keyword CONFIG.

Single Location

```
CONFIG PROHIBIT=location;
```

Multiple Single Locations

```
CONFIG PROHIBIT=location1, location2, ... ,locationn;
```

Range of Locations

```
CONFIG PROHIBIT=location1:location2;
```

where *location* is a legal location type for the part type.

See the preceding "Location Types for FPGAs" and "Location Types for CPLDs" sections. Examples of using the location types are given in "LOC".

CPLDs do not support the "Range of locations" form of PROHIBIT.

The following statement prohibits use of the site P45.

```
CONFIG PROHIBIT=P45;
```

For CLB-based Row/Column/Slice Designations

The following statement prohibits use of the CLB located in Row 6, Column 8.

```
CONFIG PROHIBIT=CLB_R6C8;
```

The following statement prohibits use of the site TBUF_R5C2.2.

```
CONFIG PROHIBIT=TBUF_R5C2.2;
```

For Slice-based XY Coordinate Designations

The following statement prohibits use of the slice at the SLICE_X6Y8 site.

```
CONFIG PROHIBIT=SLICE_X6Y8;
```

The following statement prohibits use of the TBUF at the TBUF_X6Y2 site.

```
CONFIG PROHIBIT=TBUF_X6Y2;
```

XCF

Not applicable.

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

In the Ports tab, click Prohibit I/O Locations and then fill out the Prohibit I/O Locations dialog box.

PCF

For single or multiple single locations:

```
COMP "comp_name" PROHIBIT = [SOFT] "site_group"..."site_group";
COMPGRP "group_name" PROHIBIT = [SOFT] "site_group"..."site_group";
MACRO "name" PROHIBIT = [SOFT] "site_group"..."site_group";
```

For a range of locations:

```
COMP "comp_name" PROHIBIT = [SOFT] "site_group"... "site_group";
COMPGRP "group_name" PROHIBIT = [SOFT] "site_group"... "site_group";
MACRO "name" PROHIBIT = [SOFT] "site_group"..."site_group";
```

- *site_group* is one of the following
  - **SITE "***site_name***"**
  - **SITEGRP "***site_group_name***"**
- *site_name* is a component site (that is, a CLB or IOB location)

Floorplanner

The Floorplanner supports PROHIBIT. For further details, see the Prohibit command section in the Floorplanner online help.

PACE

The Pin Assignments Editor can be used to set PROHIBIT. For details, see the Prohibit Mode command section in the PACE online help.

FPGA Editor

The FPGA Editor supports the PROHIBIT. See the Prohibit Constraint topic in the FPGA Editor online help. The constraint is written to the PCF file by the Editor.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

PULLDOWN

PULLDOWN Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

PULLDOWN Applicable Elements

Input, tri-state outputs, and bidirectional pad nets

PULLDOWN Description

PULLDOWN is a basic mapping constraint. It guarantees a logic Low level to allow 3-stated nets to avoid floating when not being driven.

Note: KEEPER, PULLUP, and PULLDOWN are only valid on pad NETs, not on INSTs of any kind.

PULLDOWN Propagation Rules

PULLDOWN is a net constraint. Any attachment to a design element is illegal.

PULLDOWN Syntax Examples

Schematic

Attach to a pad net.

Attribute Name—PULLDOWN

Attribute Values—TRUE, FALSE

VHDL

Before using PULLDOWN, declare it with the following syntax:

```
attribute pulldown: string;
```

After PULLDOWN has been declared, specify the VHDL constraint as follows:

```
attribute pulldown of signal_name: signal is “yes”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute pulldown [of] signal_name [is] “yes”;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

The following statement configures the IO to use a PULLDOWN.

```
NET "pad_net_name" PULLDOWN;
```

XCF

```
BEGIN MODEL “entity_name”
 NET  "signal_name" pulldown=true;
END;
```

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

In the Ports tab grid with I/O Configuration Options checked, click the PULLUP/PULLDOWN column in the row with the desired port name and choose PULLDOWN from the drop down list.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

PULLUP

PULLUP Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	Yes*
CoolRunner-II	Yes
* Inputs only.	

PULLUP Applicable Elements

Input, tri-state outputs, and bidirectional pad nets

PULLUP Description

PULLUP is a basic mapping constraint. It guarantees a logic High level to allow 3-stated nets to avoid floating when not being driven.

KEEPER, PULLUP, and PULLDOWN are only valid on pad NETs, not on INSTs of any kind.

Note: For CoolRunner-II designs, the use of KEEPER and the use of PULLUP are mutually exclusive across the whole device.

PULLUP Propagation Rules

PULLUP is a net constraint. Any attachment to a design element is illegal.

PULLUP Syntax Examples

Schematic

Attach to a pad net.

Attribute Name—PULLUP

Attribute Values—TRUE, FALSE

VHDL

Before using PULLUP, declare it with the following syntax:

```
attribute pullup: string;
```

After PULLUP has been declared, specify the VHDL constraint as follows:

```
attribute pullup of signal_name: signal is “yes”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute pullup [of] signal_name [is] “yes”;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

```
XILINX PROPERTY 'PULLUP mysignal';
```

UCF/NCF

The following statement configures the IO to use a PULLUP.

```
NET "pad_net_name" PULLUP;
```

XCF

```
BEGIN MODEL “entity_name”
 NET  "signal_name" pullup=true;
END;
```

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

In the Ports tab grid with I/O Configuration Options checked, click the PULLUP/PULLDOWN column in the row with the desired port name and choose PULLUP from the drop down list.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

PWR_MODE

PWR_MODE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	No
Spartan-3E	No
Virtex-II	No
Virtex-II Pro	No
Virtex-II Pro X	No
Virtex-4	No
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	No
CoolRunner-II	No

PWR_MODE Applicable Elements

- Nets
- Any instance

PWR_MODE Description

PWR_MODE is an advanced fitter constraint. It defines the mode, Low power or High performance (standard power), of the macrocell that implements the tagged element.

If the tagged function is collapsed forward into its fanouts, PWR_MODE is not applied.

PWR_MODE Propagation Rules

When attached to a net, PWR_MODE attaches to all applicable elements that drive the net.

When attached to a design element, PWR_MODE propagates to all applicable elements in the hierarchy within the design element.

PWR_MODE Syntax Examples

Schematic

Attach to a net or an instance.

Attribute Name—PWR_MODE

Attribute Values—LOW, STD

VHDL

Before using PWR_MODE, declare it with the following syntax:

```
attribute pwr_mode: string;
```

After PWR_MODE has been declared, specify the VHDL constraint as follows:

```
attribute pwr_mode of {signal_name|component_name|label_name}:
{signal|component|label} is “{LOW|STD}”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
 // synthesis attribute pwr_mode [of]
{module_name|instance_name|signal_name} [is] {LOW|STD};
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

```
XILINX PROPERTY 'pwr_mode={low|std} mysignal';
```

UCF/NCF

The following statement specifies that the macrocell that implements the net $SIG_0 will be in Low power mode.

```
NET “$1187/$SIG_0” PWR_MODE=LOW;
```

XCF

```
BEGIN MODEL “entity_name”
 NET  "signal_name" PWR_MODE={LOW|STD};
 INST "instance_name" PWR_MODE={LOW|STD};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

RAM_EXTRACT

RAM_EXTRACT Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

RAM_EXTRACT Applicable Elements

You can apply RAM_EXTRACT globally, or to an entity, module, or signal.

RAM_EXTRACT Description

RAM_EXTRACT is a synthesis constraint. It enables or disables RAM macro inference. Allowed values are YES and NO (TRUE and FALSE ones are available in XCF as well). By default, RAM inference is enabled (**YES**).

RAM_EXTRACT Propagation Rules

Applies to the entity, module, or signal to which it is attached.

RAM_EXTRACT Syntax Examples

Schematic

Not applicable.

VHDL

Before using RAM_EXTRACT, declare it with the following syntax:

```
attribute ram_extract: string;
```

After RAM_EXTRACT has been declared, specify the VHDL constraint as follows:

```
attribute ram_extract of {signal_name|entity_name}: {signal|entity} is
“yes”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
 // synthesis attribute ram_extract [of] {module_name|signal_name} [is]
yes;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL “entity_name” ram_extract={true|false|yes|no};


BEGIN MODEL “entity_name”
 NET “signal_name” ram_extract={true|false|yes|no};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-ram_extract** command line option of the **run** command. Following is the basic syntax:

```
-ram_extract {YES|NO}
```

The default is **YES**.

Project Navigator

Set globally with the RAM Extraction option in the HDL Options tab of the Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

RAM_STYLE

RAM_STYLE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

RAM_STYLE Applicable Elements

You can apply RAM_STYLE globally or to an entity, module, or signal.

RAM_STYLE Description

RAM_STYLE is a synthesis constraint. It controls the way the macrogenerator implements the inferred RAM macros. Allowed values are **AUTO**, **BLOCK** and **DISTRIBUTED**. The default value is **AUTO**, meaning that XST looks for the best implementation for each inferred RAM. The implementation style can be manually forced to use block RAM or distributed RAM resources available in the Virtex and Spartan-II series.

RAM_STYLE Propagation Rules

Applies to the entity, module, or signal to which it is attached.

RAM_STYLE Syntax Examples

Schematic

Not applicable.

VHDL

Before using RAM_STYLE, declare it with the following syntax:

```
attribute ram_style: string;
```

After RAM_STYLE has been declared, specify the VHDL constraint as follows:

```
attribute ram_style of {signal_name|entity_name}: {signal|entity} is
"{auto|block|distributed}";
```

The default value is **AUTO**.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute ram_style [of] {module_name|signal_name} [is]
{auto|block|distributed};
```

The default value is **AUTO**.

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL "entity_name" ram_style={auto|block|distributed};

BEGIN MODEL "entity_name"
 NET "signal_name"  ram_style={auto|block|distributed};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-ram_style** command line option of the **run** command. Following is the basic syntax:

```
-ram_style {AUTO|DISTRIBUTED|BLOCK}
```

The default is **AUTO**.

Project Navigator

Set globally with the RAM Style option in the HDL Options tab of the Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

REG

REG Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	No
Spartan-3E	No
Virtex-II	No
Virtex-II Pro	No
Virtex-II Pro X	No
Virtex-4	No
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

REG Applicable Elements

Registers

REG Description

REG is a basic fitter constraint. It specifies how a register is to be implemented in the CPLD macrocell.

REG Propagation Rules

When attached to a design element, REG propagates to all applicable elements in the hierarchy within the design element.

REG Syntax Examples

Schematic

Attach to a flip-flop instance or macro containing flip-flops.

Attribute Name—REG

Attribute Values—CE, TFF

VHDL

Before using REG, declare it with the following syntax:

```
attribute reg: string;
```

After REG has been declared, specify the VHDL constraint as follows:

```
attribute reg of signal_name: signal is “{CE|TFF}”;
```

See the UCF section for descriptions of CE and TFF.

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
 // synthesis attribute reg [of] {signal_name|instance_name} [is]
{CE|TFF};
```

See the UCF section for descriptions of CE and TFF.

For a detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

```
XILINX PROPERTY 'reg={ce|tff} mysignal';
```

UCF/NCF

The basic UCF syntax is:

```
INST “instance_name” REG = {CE | TFF};
```

where

- CE, when applied to a flip-flop primitive with a CE input, forces the CE input to be implemented using a clock enable product term in the macrocell. Normally the fitter only uses the register CE input if all logic on the CE input can be implemented using the single CE product term. Otherwise the fitter decomposes the CE input into the D (or T) logic expression unless REG=CE is applied. CE product terms are not available in XC9500 devices (REG=CE is ignored). In XC9500XL and XC9500XV devices, the CE product term is only available for registers that do not use both the CLR and PRE inputs.
- TFF indicates that the register is to be implemented as a T-type flip-flop in the CPLD macrocell. If applied to a D-flip-flop primitive, the D-input expression is transformed to T-input form and implemented with a T-flip-flop. Automatic transformation between D and T flip-flops is normally performed by the CPLD fitter.

The following statement specifies that the CE pin input be implemented using the clock enable product term of the XC9500XL or XC9500XV macrocell.

```
INST “Q1” REG=CE;
```

XCF

```
BEGIN MODEL “entity_name”
 NET  "signal_name" REG={CE|TFF};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

REGISTER_BALANCING

REGISTER_BALANCING Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

REGISTER_BALANCING Applicable Elements

You can apply REGISTER_BALANCING globally or to an entity, module, or signal.

REGISTER_BALANCING Description

The main goal of register balancing is to move flip-flops and latches across logic to increase clock frequency. There are two categories of register balancing:

- Forward Register Balancing will move a set of flip-flops that are at the inputs of a LUT to a single flip-flop at its output.

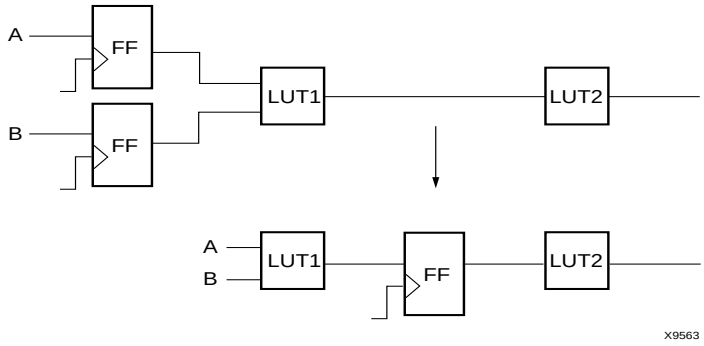


Figure 108-1: **Forward Register Balancing**

- Backward Register Balancing will move a flip-flop which is at the output of a LUT to a set of flip-flops at its inputs.

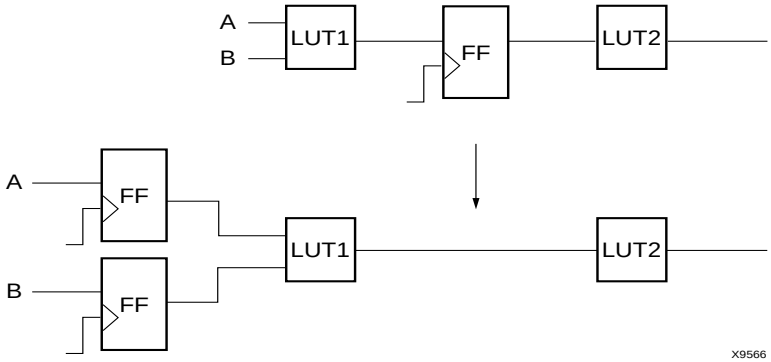


Figure 108-2: **Backward Register Balancing**

As a consequence the number of flip-flops in the design can be increased or decreased.

This constraint may have the following values : **yes**, **no**, **forward**, and **backward**. (**TRUE** and **FALSE** ones are available in XCF as well). The default is **no**, meaning that XST will not perform flip-flop retiming. **Yes** means that both forward and backward retiming are possible. **Forward** means that only forward retiming is allowed, while **backward** means that only backward retiming is allowed.

This constraint can be applied:

- Globally to the entire design via command line or GUI
- To an entity or module
- To a signal corresponding to the flip-flop description (RTL)
- Flip-flop instance
- Primary Clock Signal. In this case the register balancing will be performed only for FFs synchronized by this clock.

There are two additional constraints, called MOVE_FIRST_STAGE and MOVE_LAST_STAGE, that control the register balancing process.

Several constraints have their influence on the register balancing process:

- Hierarchy Treatment
  - Preserved, then flip-flops will be moved only inside the block boundaries.
  - Flattened, then flip-flops may leave the block boundaries.
- IOB=TRUE

  Register Balancing will be not applied to the flip-flops having this property.
- KEEP

  If applied to the output flip-flop signal, then the flip-flop will not be moved forward.

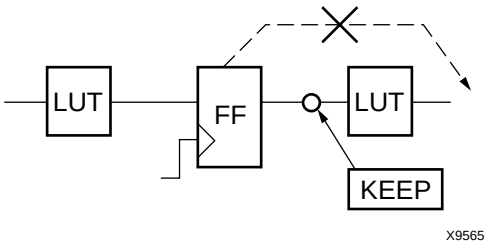


Figure 108-3: **Applied to the Output Flip-Flop Signal**

- If applied to the input flip-flop signal, then FF will not be moved backward.

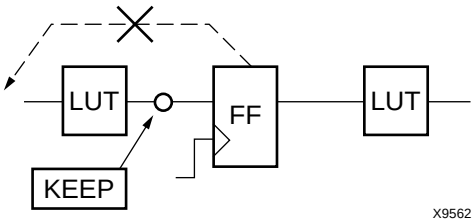


Figure 108-4: **Applied to the Input Flip-Flop Signal**

- If applied to both the input and output of the flip-flop, then it is equivalent to -register_balancing=no.
- When moving flip-flops, XST applies the following naming conventions:
- Backward Register Balancing: the new flip-flop will have the same name as the original flip-flop with an indexed suffix.

  *OriginalFFName*_BRB*Id*
- Forward Register Balancing: when replacing several flip-flops by one, select the name based on the name of the LUT across which the flip-flops are moving. The flip-flop name will be:

  *LutName*_BRB*Id*

REGISTER_BALANCING Propagation Rules

Applies to the entity, module, or signal to which it is attached.

REGISTER_BALANCING Syntax Examples

Schematic

Not applicable.

VHDL

Before using REGISTER_BALANCING, declare it with the following syntax:

```
attribute register_balancing: string;
```

After REGISTER_BALANCING has been declared, specify the VHDL constraint as follows:

```
attribute register_balancing of {signal_name|entity_name}:
{signal|entity} is "{yes|no|foward|backward}";
```

The default value is NO.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute register_balancing [of]
{module_name|signal_name} [is] {yes|no|foward|backward};
```

The default value is NO.

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL "entity_name" register_balancing={yes|no|true|false|forward|
backward};


BEGIN MODEL "entity_name"
 NET "primary_clock_signal"
 register_balancing={yes|no|true|false|forward|backward};
 INST "instance_name"  register_balancing={yes|no|true|false|forward|
 backward};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-register_balancing** command line option of the **run** command. Following is the basic syntax:

```
-register_balancing {YES|NO|FORWARD|BACKWARD}
```

The default is **NO**.

Project Navigator

Set with the Register Balancing option in the Xilinx Specific Options tab of the Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

REGISTER_DUPLICATION

REGISTER_DUPLICATION Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

REGISTER_DUPLICATION Applicable Elements

REGISTER_DUPLICATION can be only applied globally or to an entity or module.

REGISTER_DUPLICATION Description

REGISTER_DUPLICATION is a synthesis constraint. It enables or disables register replication. Allowed values are **YES** and **NO**. (**TRUE** and **FALSE** ones are available in XCF as well). The default is **YES**, and means that register replication is enabled, and is performed during timing optimization and fanout control.

REGISTER_DUPLICATION Propagation Rules

Applies to the entity or module to which it is attached.

REGISTER_DUPLICATION Syntax Examples

Schematic

Not applicable.

VHDL

Before REGISTER_DUPLICATION can be used, it must be declared with the following syntax:

```
attribute register_duplication: string;
```

After REGISTER_DUPLICATION has been declared, specify the VHDL constraint as follows:

```
attribute register_duplication of entity_name: entity is “yes”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute register_duplication [of] module_name [is]
“yes”;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL “entity_name” register_duplication={true|false|yes|no};

BEGIN MODEL “entity_name”
 NET “signal_name”  register_duplication={true|false|yes|no};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Specify globally with the Register Duplication option in the Xilinx Specific Options tab of the Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

REGISTER_POWERUP

REGISTER_POWERUP Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

REGISTER_POWERUP Applicable Elements

Signals and types

REGISTER_POWERUP Description

XST will not automatically figure out and enforce register power-up values. You must explicitly specify them if needed with REGISTER_POWERUP. This XST synthesis constraint can be assigned to a VHDL enumerated type, or it may be directly attached to a VHDL signal or a Verilog register node through a VHDL attribute or Verilog meta comment. The constraint value may be a binary string or a symbolic code value.

REGISTER_POWERUP Propagation Rules

Applies to the signal or type to which it is attached.

REGISTER_POWERUP Syntax Examples

Schematic

Not applicable.

VHDL

Following are some examples of REGISTER_POWERUP.

Example 1

The register is defined with a predefined VHDL type such as std_logic_vector. The constraint value is necessarily a binary code.

```
signal myreg : std_logic_vector (3 downto 0);
attribute register_powerup of myreg : signal is "0001";
```

Example 2

The register is defined with an enumerated type (symbolic state machine). The constraint is attached to the signal and its value is one of the symbolic states defined. Actual power-up code will differ depending on the way the state machine is encoded.

```
type state_type is (s1, s2, s3, s4, s5);
signal state1 : state_type;
attribute register_powerup of state1 : signal is "s2";
```

Example 3

The constraint is attached to an enumerated type. All registers defined with that type inherit the constraint.

```
type state_type is (s1, s2, s3, s4, s5);
attribute register_powerup of state_type : type is "s1";
signal state1, state2 : state_type;
```

Example 4

For enumerated type objects, the power-up value may also be defined as a binary code. However, if automatic encoding is enabled and leads to a different encoding scheme (in particular a different code width), the power-up value will be ignored.

```
type state_type is (s1, s2, s3, s4, s5);
attribute enum_encoding of state_type : type is "001 011 010 100 111";
attribute register_powerup of state_type : type is "100";
signal state1 : state_type;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

```
//synthesis attribute register_powerup [of] {signal_name} [is] value;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
BEGIN MODEL "entity_name"
 NET "signal_name" register_powerup="string";
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

RESOURCE_SHARING

RESOURCE_SHARING Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

RESOURCE_SHARING Applicable Elements

You can apply RESOURCE_SHARING globally or to design elements.

RESOURCE_SHARING Description

RESOURCE_SHARING is a synthesis constraint. It enables or disables resource sharing of arithmetic operators. Allowed values are **YES** (check box is checked) and **NO** (check box is not checked). (**TRUE** and **FALSE** ones are available in XCF as well). By default, resource sharing is enabled.

RESOURCE_SHARING Propagation Rules

Applies to the entity or module to which it is attached.

RESOURCE_SHARING Syntax Examples

Schematic

Not applicable.

VHDL

Before RESOURCE_SHARING can be used, it must be declared with the following syntax:

```
attribute resource_sharing: string;
```

After RESOURCE_SHARING has been declared, specify the VHDL constraint as follows:

```
attribute resource_sharing of entity_name: entity is “yes”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute resource_sharing [of] module_name [is] “yes”;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL “entity_name” resource_sharing={yes|no|true|false};

BEGIN MODEL “entity_name”
  NET “signal_name” resource_sharing={yes|no|true|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-resource_sharing** command line option of the **run** command. Following is the basic syntax:

```
-resource_sharing {YES|NO}
```

The default is **YES**.

Project Navigator

Set RESOURCE_SHARING globally with the Resource Sharing option in the HDL Options tab of the Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

RESYNTHESIZE

RESYNTHESIZE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

RESYNTHESIZE Applicable Elements

RESYNTHESIZE can be only applied to design elements.

RESYNTHESIZE Description

RESYNTHESIZE is a synthesis constraint. This constraint is related to incremental synthesis flow and to INCREMENTAL_SYNTHESIS. Please refer to the INCREMENTAL_SYNTHESIS constraint section for more information. RESYNTHESIZE forces or prevents resynthesis of an entity or module in the incremental synthesis mode. Allowed values are YES and NO (TRUE and FALSE ones are available in XCF as well). No global resynthesize option is available.

RESYNTHESIZE Propagation Rules

Applies to the entity or module to which it is attached.

RESYNTHESIZE Syntax Examples

Schematic

Not applicable.

VHDL

Before RESYNTHESIZE can be used, it must be declared with the following syntax:

```
attribute resynthesize: string;
```

After RESYNTHESIZE has been declared, specify the VHDL constraint as follows:

```
attribute resynthesize of entity_name: entity is “yes”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute resynthesize [of] module_name [is] “yes”;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL “entity_name” resynthesize={true|false|yes|no};
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

RLOC

RLOC Architecture Support

The numbers in the second column indicate supported elements. See the next section.

Architecture	Supported/Unsupported
Virtex	1, 3, 4, 5, 6, 7
Virtex-E	1, 2, 3, 4, 5, 6, 7
Spartan-II	1, 3, 4, 5, 6, 7
Spartan-IIE	1, 2, 3, 4, 5,6, 7
Spartan-3	1, 2, 3, 5, 6, 7
Spartan-3E	1, 2, 3, 5, 6, 7
Virtex-II	1, 3, 4, 5, 6, 7
Virtex-II Pro	1, 3, 4, 5, 6, 7
Virtex-II Pro X	1, 3, 4, 5, 6, 7
Virtex-4	1, 2, 3, 5, 6, 7
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

RLOC Applicable Elements

1. Registers
2. ROM
3. RAMS, RAMD
4. BUFT (Can only be used if the associated RPM has an RLOC_ORIGIN that causes the RLOC values in the RPM to be changed to LOC values.)
5. LUTs, MUXF5, MUXF6, MUXCY, XORCY, MULT_AND, SRL16, SRL16E, MUXF7 (for Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X only), MUXF8 (for Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4 only)
6. Block RAMs
7. Multipliers

RLOC Description

Relative location (RLOC) is a basic mapping and placement constraint. It is also a synthesis constraint. RLOC constraints group logic elements into discrete sets and allow you to define the location of any element within the set relative to other elements in the set, regardless of eventual placement in the overall design.

For Virtex, Virtex-E, Spartan-II,Virtex-4, and Spartan-IIE, the RLOC constraint must include the extension that defines in which of the two slices of a CLB the element will be placed (.S0, .S1).

For Virtex-II, Virtex-II Pro, and Virtex-II Pro X, and Spartan-3, the RLOC constraint is specified using the slice-based XY coordinate system.

Benefits and Limitations of RLOC Constraints

RLOC constraints allow you to place logic blocks relative to each other to increase speed and use die resources efficiently. They provide an order and structure to related design elements without requiring you to specify their absolute placement on the FPGA die. They allow you to replace any existing hard macro with an equivalent that can be directly simulated.

In the Unified Libraries, you can use RLOC constraints with BUFT- and CLB-related primitives, that is, FMAP. You can also use them on non-primitive macro symbols. There are some restrictions on the use of RLOC constraints on BUFT symbols; for details, see "Set Modifiers". You cannot use RLOC constraints with decoders or clocks. LOC constraints, on the other hand, can be used on all primitives: BUFTs, CLBs, IOBs, decoders, and clocks.

The following symbols (primitives) accept RLOCs.

- Registers
- ROM
- RAMS, RAMD
- BUFT
- LUTs, MUXCY, XORCY, MULT_AND, SRL16, SRL16E

Guidelines for Specifying Relative Locations

There are two different coordinate designations:

- Virtex, Virtex-E, Spartan-II, and Spartan-IIE use the CLB-based coordinate system.
- Virtex-II, Virtex-II Pro, Virtex-II Pro X, Virtex-4, and Spartan-3 use the slice-based coordinate system.

CLB-based Row/Column/Slice Designations

For all architectures except Virtex-II, Virtex-II Pro, and Virtex-II Pro X, Virtex-4, and Spartan-3, the general syntax for assigning elements to relative locations is

RLOC=[*element*]**R***m***C***n*[*.extension*]

where

- *m* and *n* are relative row numbers and column numbers, respectively
- *extension* uses the LOC extension syntax and can take all the values that are available with the absolute LOC syntax: S0, S1, 0, 1, 2, and 3 as appropriate for the architecture and element the RLOC is attached to.

The extension is required for Virtex, Virtex-E, Spartan-II, and Spartan-IIE designs to specify the spatial relationship of the objects in the RPM (.S0, .S1).

The row and column numbers can be any positive or negative integer including zero. Absolute die locations, in contrast, cannot have zero as a row or column number. Because row and column numbers in RLOC constraints define only the order and relationship between design elements and not their absolute die locations, their numbering can include zero or negative numbers. Even though you can use any integer in numbering rows and columns for RLOC constraints, it is recommended that you use small integers for clarity and ease of use.

It is not the absolute values of the row and column numbers that is important in RLOC specifications but their relative values or differences. For example, if design element A has an RLOC=R3C4 constraint and design element B has an RLOC=R6C7 constraint, the absolute values of the row numbers (3 and 6) are not important in themselves. However, the difference between them is important; in this case, 3 (6 -3) specifies that the location of design element B is three rows down from the location of design element A.

To capture this information, a normalization process is used and column-wise the design element B is 3 (7-4) columns on the right of element A. In the example just given, normalization would reduce the RLOC on design element A to R0C0, and the RLOC on design element B to R3C3.

In CLB-based programs, row / column rows are numbered in increasing order from top to bottom, and columns are numbered in increasing order from left to right. RLOC constraints follow this numbering convention.

Figure 113-1 demonstrates the use of RLOC constraints.

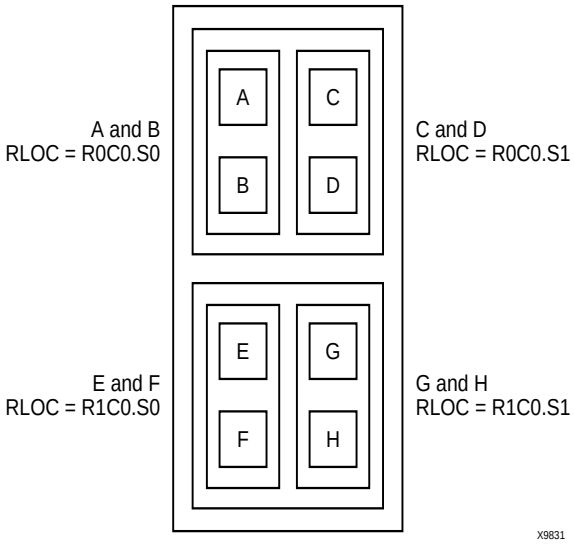


Figure 113-1: **RLOC Specifications for Eight Flip-Flop Primitives for Virtex, Virtex-E, Spartan-II, and Spartan-IIE Architectures**

Slice-based XY Coordinate Designations

For Virtex-II, Virtex-II Pro, and Virtex-II Pro X, Virtex-4, and Spartan-3, the general syntax for assigning elements to relative locations is

RLOC=X*m*Y*n*

where

- *m* and *n* are the relative X-axis (left / right) value and the relative Y-axis (up / down) value, respectively
- the X and Y numbers can be any positive or negative integer including zero

Because the X and Y numbers in RLOC constraints define only the order and relationship between design elements and not their absolute die locations, their numbering can include negative numbers. Even though you can use any integer for RLOC constraints, it is recommended that you use small integers for clarity and ease of use.

It is not the absolute values of the X and Y numbers that is important in RLOC specifications but their relative values or differences. For example, if design element A has an RLOC=X3Y4 constraint and design element B has an RLOC=X6Y7 constraint, the absolute values of the X numbers (3 and 6) are not important in themselves. However, the difference between them is important; in this case, 3 (6 -3) specifies that the location of design element B is three slices away from the location of design element A.

To capture this information, a normalization process is used and y coordinate-wise, element B is 3 (7-4) slices above element A. In the example just given, normalization would reduce the RLOC on design element A to X0Y0, and the RLOC on design element B to X3Y3.

In Virtex-II, Virtex-II Pro, and Virtex-II Pro X, Virtex-4, and Spartan-3, slices are numbered on an XY grid beginning in the lower left corner of the chip. X ascends in value horizontally to the right. Y ascends in value vertically up. RLOC constraints follow the cartesian-based convention.

Figure 113-2 demonstrates the use of RLOC constraints. In (a) in Figure 113-2 four flip-flop primitives named A, B, C, and D are assigned RLOC constraints as shown. These RLOC constraints require each flip-flop to be placed in a different slice with the slices stacked in the order shown — A below B, C, and D.

If you wish to place more than one of these flip-flop primitives per slice, you can specify the RLOCs as shown in (b) in Figure 113-2. The arrangement in the figure requires that A

and B be placed in a single slice and that C and D be placed in another slice immediately to the right of the AB slice.

Figure 113-2: **Different RLOC Specifications for Four Flip-flop Primitives for a Virtex-II, Virtex-II Pro, and Virtex-II Pro X, Virtex-4, and Spartan-3, Design**

RLOC Sets

RLOC constraints give order and structure to related design elements. This section describes RLOC sets, which are groups of related design elements to which RLOC constraints have been applied. For example, the eight flip-flops in Figure 113-1 and the four flip-flops in Figure 113-2 are related by RLOC constraints and form a set. Elements in a set are related by RLOC constraints to other elements in the same set. Each member of a set must have an RLOC constraint, which relates it to other elements in the same set. You can create multiple sets, but a design element can belong to one set only.

Sets can be defined explicitly through the use of a set parameter or implicitly through the structure of the design hierarchy.

Four distinct types of rules are associated with each set.

- Definition rules define the requirements for membership in a set.
- Linkage rules specify how elements can be linked to other elements to form a single set.
- Modification rules dictate how to specify parameters that modify RLOC values of all the members of the set.
- Naming rules specify the nomenclature of sets.

These rules are discussed in the sections that follow.

The following sections discuss three different set constraints— U_SET, H_SET, and HU_SET. Elements must be tagged with both the RLOC constraint and one of these set constraints to belong to a set.

U_SET

U_SET constraints enable you to group into a single set design elements with attached RLOC constraints that are distributed throughout the design hierarchy. The letter U in the name U_SET indicates that the set is user-defined.

U_SET constraints allow you to group elements, even though they are not directly related by the design hierarchy. By attaching a U_SET constraint to design elements, you can explicitly define the members of a set.

The design elements tagged with a U_SET constraint can exist anywhere in the design hierarchy; they can be primitive or non-primitive symbols. When attached to non-primitive symbols, the U_SET constraint propagates to all the primitive symbols with RLOC constraints that are below it in the hierarchy.

The syntax of the U_SET constraint is:

U_SET=*set_name*

where *set_name* is the user-specified identifier of the set.

All design elements with RLOC constraints tagged with the same U_SET constraint name belong to the same set. Names therefore must be unique among all the sets in the design.

H_SET

In contrast to the U_SET constraint, which you explicitly define by tagging design elements, the H_SET (hierarchy set) is defined implicitly through the design hierarchy. The combination of the design hierarchy and the presence of RLOC constraints on elements defines a hierarchical set, or H_SET set.

You are *not* able to use an H_SET constraint to tag the design elements to indicate their set membership. The set is defined automatically by the design hierarchy.

All design elements with RLOC constraints at a single node of the design hierarchy are considered to be in the same H_SET set unless they are tagged with another type of set constraint such as RLOC_ORIGIN or RLOC_RANGE. If you explicitly tag any element with an RLOC_ORIGIN, RLOC_RANGE, U_SET, or HU_SET constraint, it is removed from an H_SET set.

Most designs contain only H_SET constraints, since they are the underlying mechanism for relationally placed macros. The RLOC_ORIGIN or RLOC_RANGE constraints are discussed further in "Set Modifiers".

NGDBuild recognizes the implicit H_SET set, derives its name, or identifier, attaches the H_SET constraint to the correct members of the set, and writes them to the output file.

HU_SET

The HU_SET constraint is a variation of the implicit H_SET (hierarchy set). Like H_SET, HU_SET is defined by the design hierarchy. However, you can use the HU_SET constraint to assign a user-defined name to the HU_SET.

The syntax of the HU_SET constraint is:

HU_SET=*set_name*

where *set_name* is the identifier of the set. It must be unique among all the sets in the design.

This user-defined name is the base name of the HU_SET set. Like the H_SET set, in which the base name of "h_set" is prefixed by the hierarchical name of the lowest common ancestor of the set elements, the user-defined base name of an HU_SET set is prefixed by the hierarchical name of the lowest common ancestor of the set elements.

You must define the base names to ensure unique hierarchically qualified names for the sets before the mapper resolves the design and attaches the hierarchical names as prefixes.

The HU_SET constraint defines the start of a new set. All design elements at the same node that have the same user-defined value for the HU_SET constraint are members of the same HU_SET set. Along with the HU_SET constraint, elements can also have an RLOC constraint.

The presence of an RLOC constraint in an H_SET constraint links the element to all elements tagged with RLOCs above and below in the hierarchy. However, in the case of an HU_SET constraint, the presence of an RLOC constraint along with the HU_SET constraint on a design element does not automatically link the element to other elements with RLOC constraints at the same hierarchy level or above.

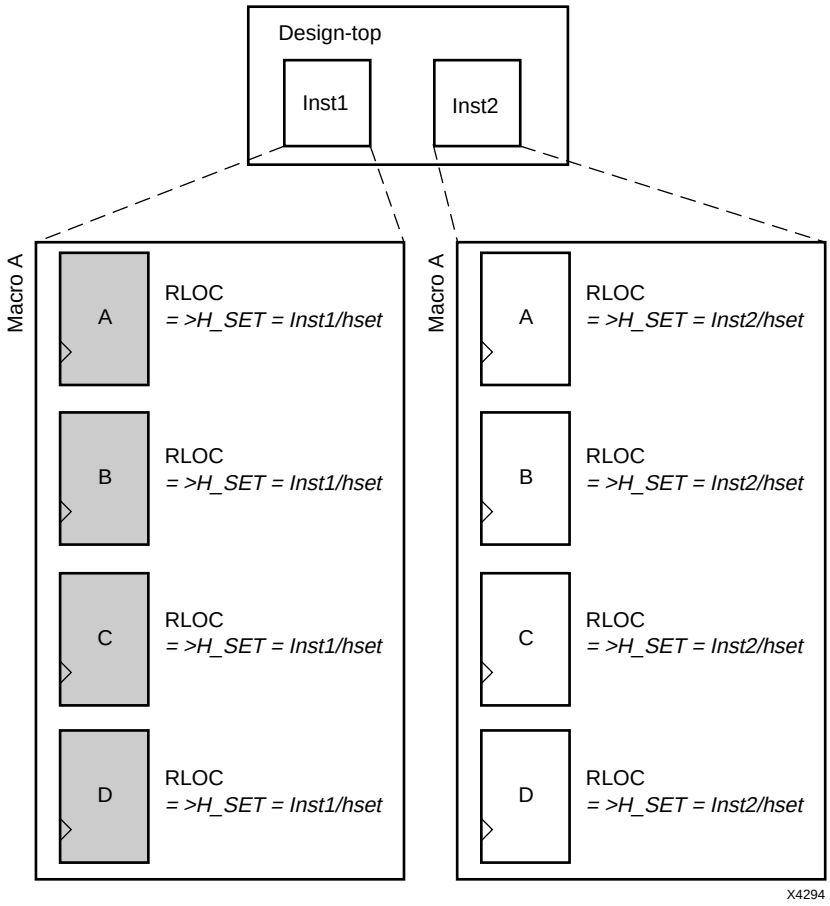


Figure 113-3: **Macro A Instantiated Twice**

Note: In Figure 113-3 and the other related figures shown in the subsequent sections, the italicized text prefixed by => is added by NGDBuild during the design flattening process. You add all other text.

Figure 113-3 demonstrates a typical use of the implicit H_SET (hierarchy set). The figure shows only the first "RLOC" portion of the constraint. In a real design, the RLOC constraint must be specified completely with RLOC=R*m*C*n* or, for Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4 RLOC=X*m*Y*n*. In this example, macro A is originally designed with RLOC constraints on four flip-flops — A, B, C, and D. The macro is then instantiated twice in the design — Inst1 and Inst2.

When the design is flattened, two different H_SET sets are recognized because two distinct levels of hierarchy contain elements with RLOC constraints. NGDBuild creates and attaches the appropriate H_SET constraint to the set members: H_SET=Inst1/h_set for the macro instantiated in Inst1, and H_SET=Inst2/h_set for the macro instantiated in Inst2. The design implementation programs place each of the two sets individually as a unit with relative ordering within each set specified by the RLOC constraints. However, the two sets are regarded to be completely independent of each other.

The name of the H_SET set is derived from the symbol or node in the hierarchy that includes all the RLOC elements. In the Figure 113-3, Inst1 is the node (instantiating macro) that includes the four flip-flop elements with RLOCs shown on the left of the figure. Therefore, the name of this H_SET set is the hierarchically qualified name of "Inst1" followed by "h_set."

The Inst1 symbol is considered the “start” of the H_SET, which gives a convenient handle to the entire H_SET and attaches constraints that modify the entire H_SET. Constraints that modify sets are discussed in “SAVE NET FLAG”.

Figure 113-3 demonstrates the simplest use of a set that is defined and confined to a single level of hierarchy. Through linkage and modification, you can also create an H_SET set that is linked through two or more levels of hierarchy.

Linkage allows you to link elements through the hierarchy into a single set. On the other hand, modification allows you to modify RLOC values of the members of a set through the hierarchy.

RLOC Set Summary

The following table summarizes the RLOC set types and the constraints that identify members of these sets.

Table 113-1: **Summary of Set Types**

Type	Definition	Naming	Linkage	Modification
U_SET= name	All elements with the same user-tagged U_SET constraint value are members of the same U_SET set.	The name of the set is the same as the user-defined name without any hierarchical qualification.	U_SET links elements to all other elements with the same value for the U_SET constraint.	U_SET is modified by applying RLOC_ORIGIN or RLOC_RANGE constraints on, at most, one of the U_SET constraint-tagged elements.
HU_SET= name	All elements with the same hierarchically qualified name are members of the same set.	The lowest common ancestor of the members is prefixed to the user-defined name to obtain the name of the set.	HU_SET links to other elements at the same node with the same HU_SET constraint value. It links to elements with RLOC constraints below.	The start of the set is made up of the elements on the same node that are tagged with the same HU_SET constraint value. An RLOC_ORIGIN or an RLOC_RANGE can be applied to, at most, one of these start elements of an HU_SET set.

RLOC Propagation Rules

RLOC is a design element constraint and any attachment to a net is illegal. When attached to a design element, RLOC propagates to all applicable elements in the hierarchy within the design element.

RLOC Syntax

For Architectures Using CLB-based Row/Column/Slice Specifications

Virtex, and Virtex-E, Spartan-II, Spartan-IIE

RLOC=R*m***C***n*.*extension*

where

- *m* and *n* are integers (positive, negative, or zero) representing relative row numbers and column numbers, respectively
- *extension* uses the LOC extension syntax as appropriate. It can take all the values that are available with the current absolute LOC syntax.

For Virtex, Virtex-E, Spartan-II and Spartan-IIE, *extension* is required to define the spatial relationships (.S0 is the right-most slice; .S1 is the left-most slice) of the objects in the RPM.

The RLOC value cannot specify a range or a list of several locations; it must specify a single location. See "RLOC Description" for more information.

For Architectures Using a Slice-based XY Coordinate System (Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4 Only)

RLOC=X*m*Y*n*

where *m* and *n* are integers (positive, negative, or zero) representing relative X and Y coordinates, respectively.

Set Linkage

The example in Figure 113-4 explains and illustrates the process of linking together elements through the design hierarchy. Again, the complete RLOC specification, RLOC=R*m*C*n* or RLOC=X*m*X*n*, is required for a real design.

Note: In this and other illustrations in this section, the sets are shaded differently to distinguish one set from another.

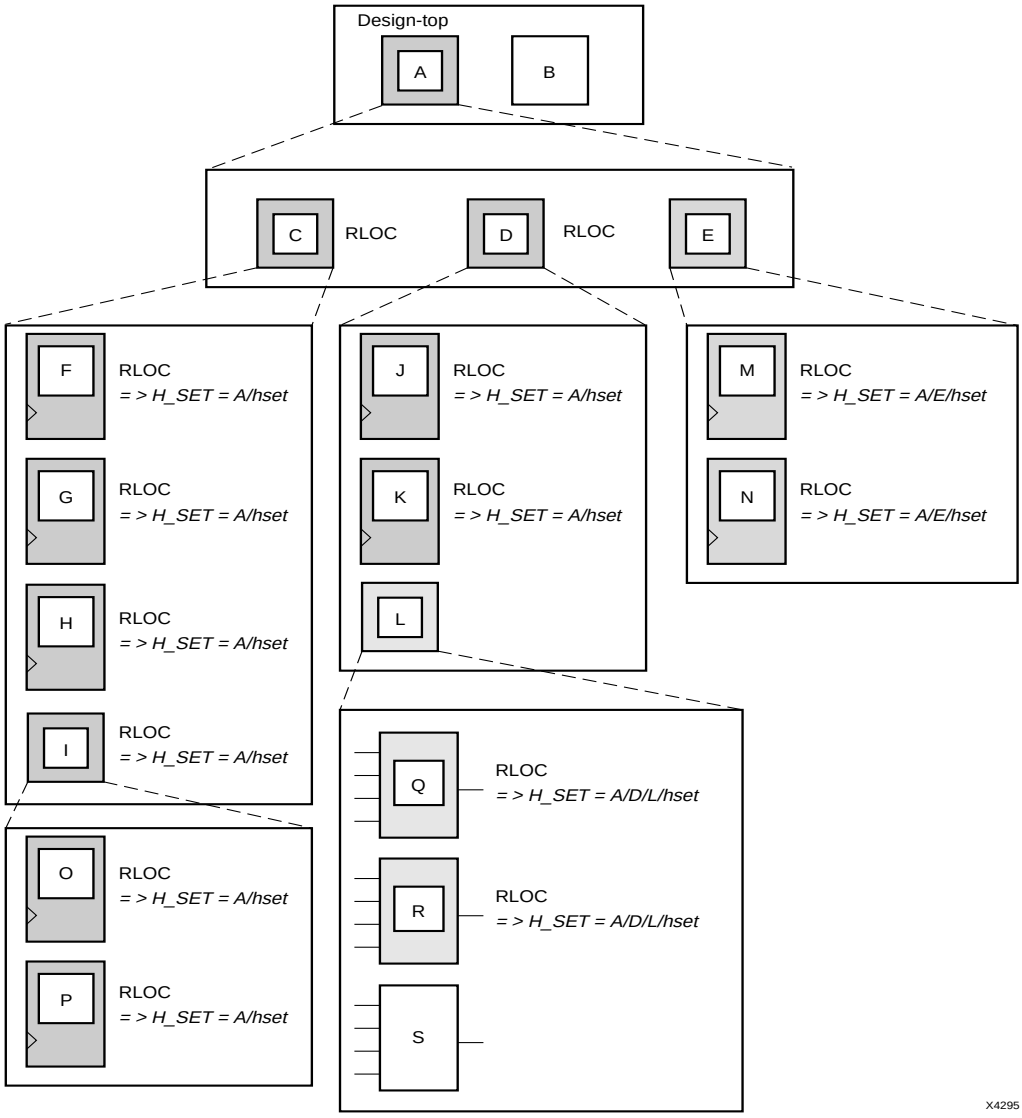


Figure 113-4: **Three H_SET Sets**

As noted previously, all design elements with RLOC constraints at a single node of the design hierarchy are considered to be in the same H_SET set unless they are assigned another type of set constraint, an RLOC_ORIGIN constraint, or an RLOC_RANGE constraint. In the Figure 113-4, RLOC constraints have been added on primitives and non-primitives C, D, F, G, H, I, J, K, M, N, O, P, Q, and R. No RLOC constraints were placed on B, E, L, or S. Macros C and D have an RLOC constraint at node A, so all the primitives below C and D that have RLOCs are members of a single H_SET set.

Furthermore, the name of this H_SET set is "A / h_set" because it is at node A that the set starts. The start of an H_SET set is the lowest common ancestor of all the RLOC-tagged constraints that constitute the elements of that H_SET set.

Because element E does not have an RLOC constraint, it is not linked to the A/h_set set. The RLOC-tagged elements M and N, which lie below element E, are therefore in their own H_SET set. The start of that H_SET set is A/E, giving it the name "A/E/h_set."

Similarly, the Q and R primitives are in their own H_SET set because they are not linked through element L to any other design elements. The lowest common ancestor for their H_SET set is L, which gives it the name "A/D/L/h_set." After the flattening, NGDBuild attaches H_SET=A/h_set to the F, G, H, O, P, J, and K primitives; H_SET=A/D/L/h_set to the Q and R primitives; and H_SET=A/E/h_set to the M and N primitives.

Consider a situation in which a set is created at the top of the design. In Figure 113-4, there would be no lowest common ancestor if macro A also had an RLOC constraint, since A is at the top of the design and has no ancestor. In this case, the base name "h_set" would have no hierarchically qualified prefix, and the name of the H_SET set would simply be "h_set."

Set Modification

The RLOC constraint assigns a primitive an RLOC value (the row and column numbers with the optional extensions), specifies its membership in a set, and links together elements at different levels of the hierarchy. In Figure 113-4, the RLOC constraint on macros C and D links together all the objects with RLOC constraints below them. An RLOC constraint is also used to modify the RLOC values of constraints below it in the hierarchy. In other words, RLOC values of elements affect the RLOC values of all other member elements of the same H_SET set that lie below the given element in the design hierarchy.

The Effect of the Hierarchy on Set Modification

The following sections describe the effect of the hierarchy on set modification for the CLB-based Row/Column/Slice designations and for the slice-based XY coordinate designations (Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4).

CLB-based Row/Column/Slice Designations

When the design is flattened, the row and column numbers of an RLOC constraint on an element are added to the row and column numbers of the RLOC constraints of the set members below it in the hierarchy. This feature gives you the ability to modify existing RLOC values in submodules and macros without changing the previously assigned RLOC values on the primitive symbols.

This modification process also applies to the optional extension field. However, when using extensions for modifications, you must ensure that inconsistent extensions are not attached to the RLOC value of a design element that may conflict with RLOC extensions placed on underlying elements.

For example, if an element has an RLOC constraint with the S0 extension, all the underlying elements with RLOC constraints must either have the same extension, in this case S0, or no extension at all; any underlying element with an RLOC constraint and an extension different from S0, such as S1, is flagged as an error.

After resolving all the RLOC constraints, extensions that are not valid on primitives are removed from those primitives. For example, if NGDBuild generates an S0 extension to be applied on a primitive after propagating the RLOC constraints, it applies the extension if and only if the primitive is a flip-flop. If the primitive is an element other than a flip-flop, the extension is ignored. Only the extension is ignored in this case, not the entire RLOC constraint.

Figure 113-5 illustrates the process of adding RLOC values down the hierarchy. The row and column values between the parentheses show the addition function performed by the mapper. The italicized text prefixed by => is added by MAP during the design resolution process and replaces the original RLOC constraint that you added. For S*n*, the value *n* is either a 1 or a 0.

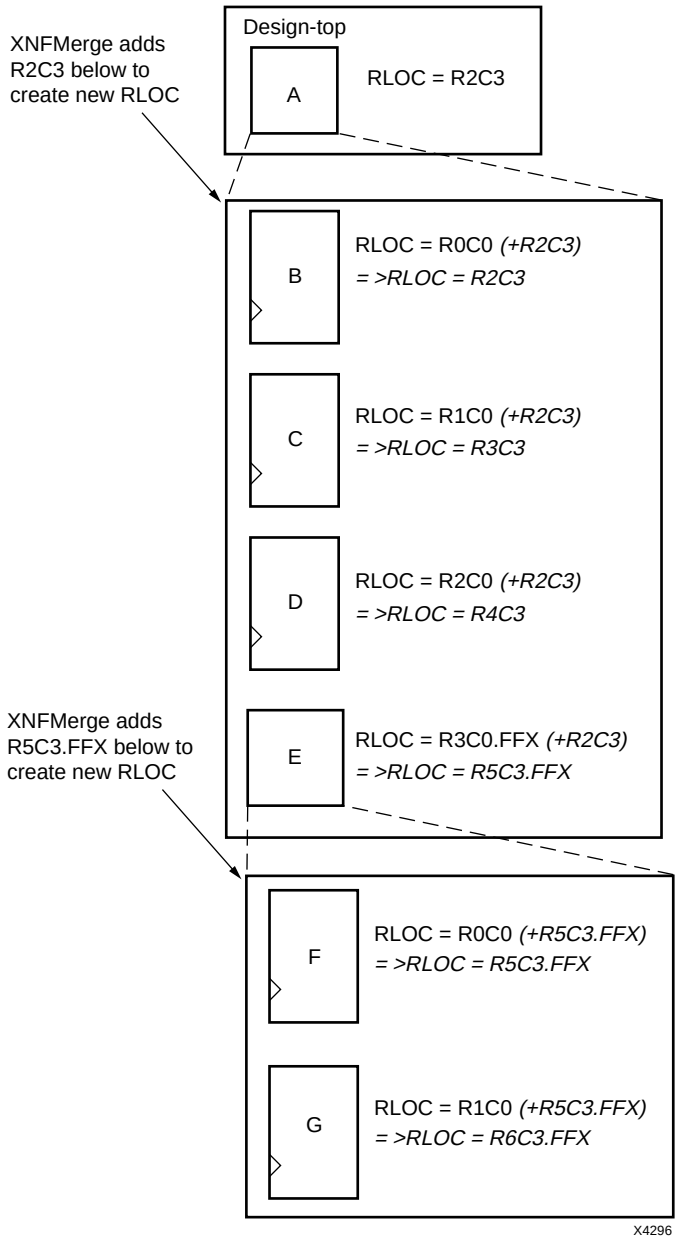


Figure 113-5: **Adding RLOC Values Down the Hierarchy (CLB-based Row/Column/Slice)**

The ability to modify RLOC values down the hierarchy is particularly valuable when instantiating the same macro more than once. Typically, macros are designed with RLOC constraints that are modified when the macro is instantiated. Figure 113-6 is a variation of the sample design in Figure 113-3. The RLOC constraint on Inst1 and Inst2 now link all the objects in one H_SET set.

Because the RLOC=R0C0 modifier on the Inst1 macro does not affect the objects below it, the mapper only adds the H_SET tag to the objects and leaves the RLOC values as they are. However, the RLOC=R0C1 modifier on the Inst2 macro causes MAP to change the RLOC values on objects below it, as well as to add the H_SET tag, as shown in the italicized text.

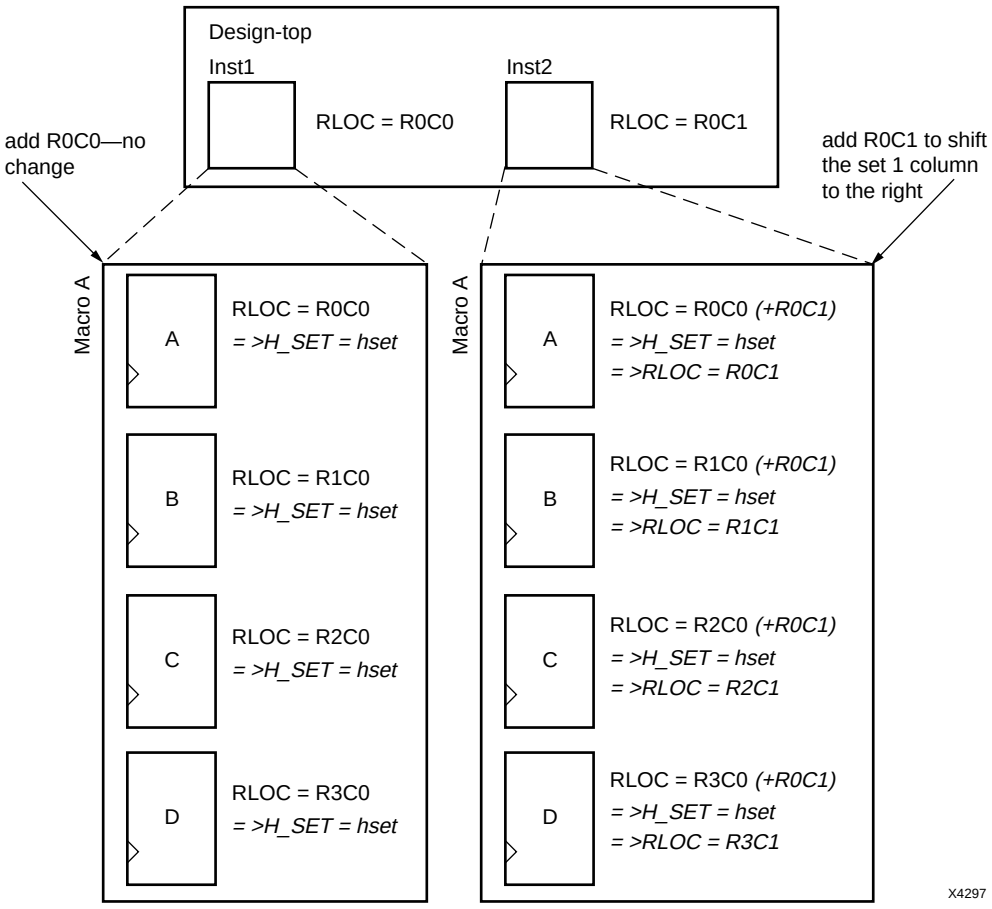


Figure 113-6: **Modifying RLOC Values of Same Macro and Linking Together as One Set (CLB-based Row/Column/Slice)**

Slice-based XY Designations

When the design is flattened, the XY values of an RLOC constraint on an element are added to the XY values of the RLOC constraints of the set members below it in the hierarchy. This feature gives you the ability to modify existing RLOC values in submodules and macros without changing the previously assigned RLOC values on the primitive symbols.

Figure 113-7 illustrates the process of adding RLOC values down the hierarchy. The row and column values between the parentheses show the addition function performed by the mapper. The italicized text prefixed by => is added by MAP during the design resolution process and replaces the original RLOC constraint that you added.

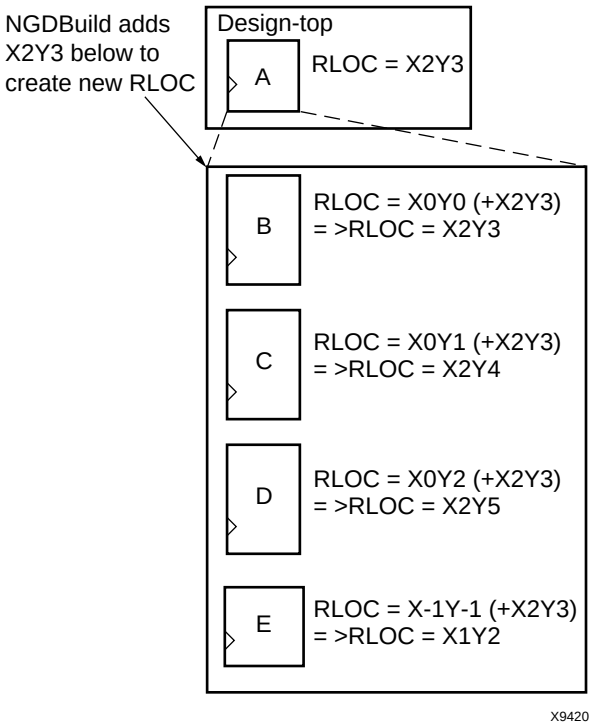


Figure 113-7: **Adding RLOC Values Down the Hierarchy Example (Slice-based XY Designations)**

The ability to modify RLOC values down the hierarchy is particularly valuable when instantiating the same macro more than once. Typically, macros are designed with RLOC constraints that are modified when the macro is instantiated. Figure 113-7 is a variation of the sample design in Figure 113-8. The RLOC constraint on Inst1 and Inst2 now link all the objects in one H_SET set.

Because the RLOC=X0Y0 modifier on the Inst1 macro does not affect the objects below it, the mapper only adds the H_SET tag to the objects and leaves the RLOC values as they are. However, the RLOC=X1Y0 modifier on the Inst2 macro causes MAP to change the RLOC values on objects below it, as well as to add the H_SET tag, as shown in the italicized text.

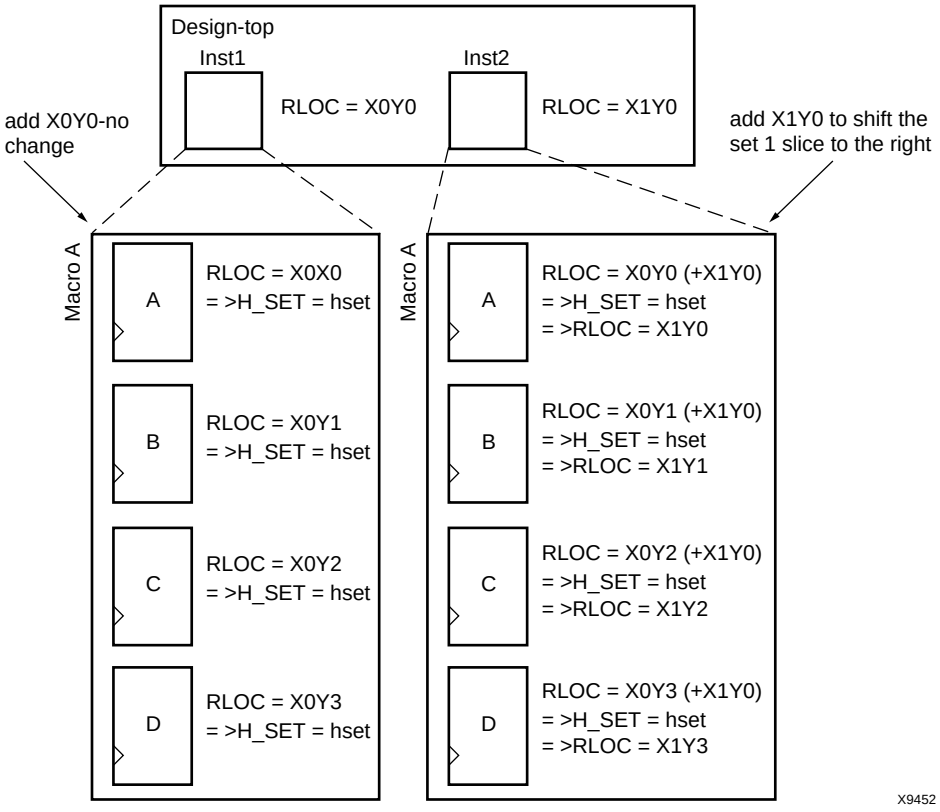


Figure 113-8: **Modifying RLOC Values of Same Macro and Linking Together as One Set (Slice-based XY Designations)**

Separating Elements from H_SET Sets

The HU_SET constraint is a variation of the implicit H_SET (hierarchy set). The HU_SET constraint defines the start of a new set. Like H_SET, HU_SET is defined by the design hierarchy. However, you can use the HU_SET constraint to assign a user-defined name to the HU_SET.

Figure 113-9 demonstrates how HU_SET constraints designate elements as set members, break links between elements tagged with RLOC constraints in the hierarchy to separate them from H_SET sets, and generate names as identifiers of these sets.

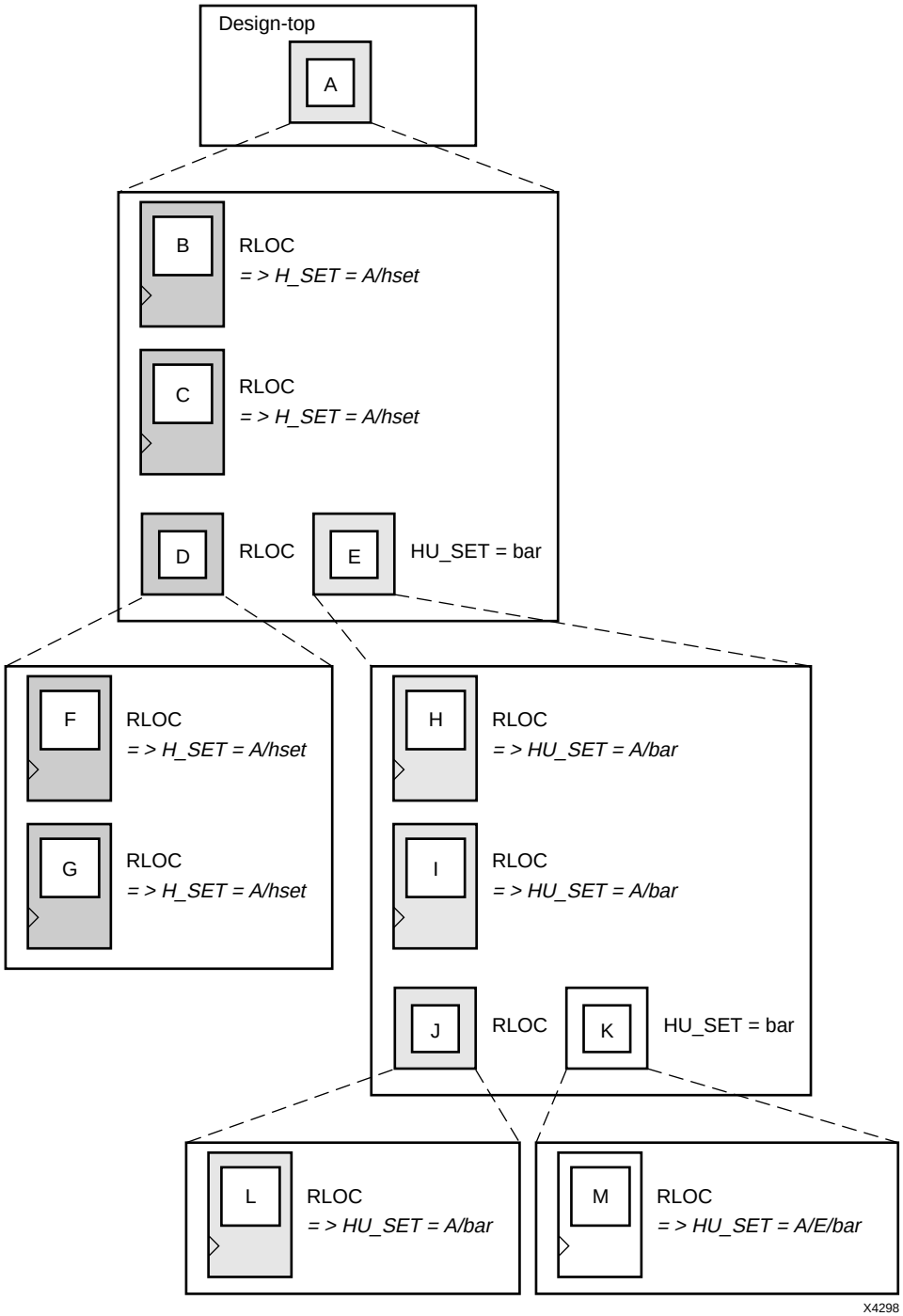


Figure 113-9: **HU_SET Constraint Linking and Separating Elements from H_SET Sets**

The user-defined HU_SET constraint on E separates its underlying design elements, namely H, I, J, K, L, and M from the implicit H_SET=A / h_set that contains primitive

members B, C, F, and G. The HU_SET set that is defined at E includes H, I, and L (through the element J).

The mapper hierarchically qualifies the name value “bar” on element E to be A/bar, since A is the lowest common ancestor for all the elements of the HU_SET set, and attaches it to the set member primitives H, I, and L. An HU_SET constraint on K starts another set that includes M, which receives the HU_SET=A/E/bar constraint after processing by the mapper.

In Figure 113-9, the same name field is used for the two HU_SET constraints, but because they are attached to symbols at different levels of the hierarchy, they define two different sets.

Figure 113-10 shows how HU_SET constraints link elements in the same node together by naming them with the same identifier. Because of the same name, “bar,” on two elements, D and E, the elements tagged with RLOC constraints below D and E become part of the same HU_SET.

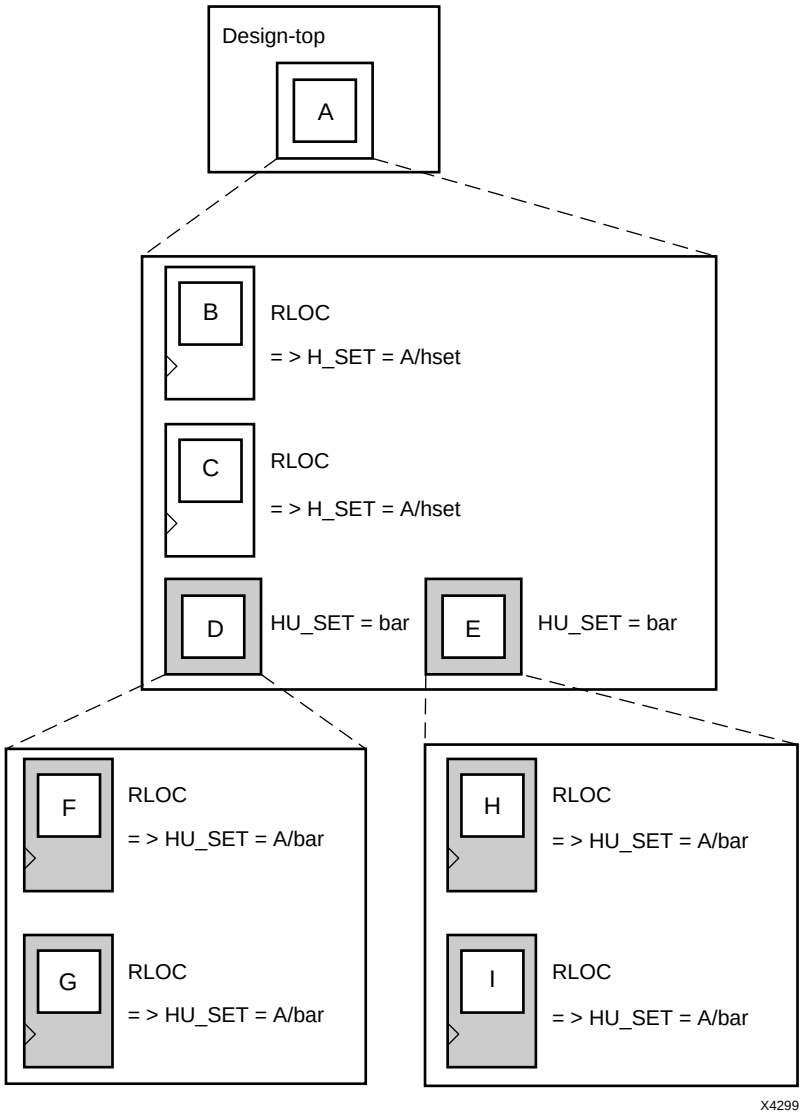


Figure 113-10: **Linking Two HU_SET Sets**

Set Modifiers

A modifier, as its name suggests, modifies the RLOC constraints associated with design elements. Since it modifies the RLOC constraints of all the members of a set, it must be applied in a way that propagates it to all the members of the set easily and intuitively. For this reason, the RLOC modifiers of a set are placed at the start of that set. The following set modifiers apply to RLOC constraints.

- RLOC

  The RLOC constraint associated with a design element modifies the values of other RLOC constraints below the element in the hierarchy of the set. Regardless of the set type, RLOC values (row, column, extension or XY values) on an element always propagate down the hierarchy and are added at lower levels of the hierarchy to RLOC constraints on elements in the same set.

- RLOC_ORIGIN (see "RLOC_ORIGIN")
- RLOC_RANGE (see "RLOC_RANGE")

Using RLOCs with Xilinx Macros

Xilinx-supplied flip-flop macros include an RLOC=R0C0 constraint on the underlying primitive, which allows you to attach an RLOC to the macro symbol. (For Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X, and Virtex-4 the macros include an RLOC=X0Y0 constraint.) This symbol links the underlying primitive to the set that contains the macro symbol.

Simply attach an appropriate RLOC constraint to the instantiation of the actual Xilinx flip-flop macro. The mapper adds the RLOC value that you specified to the underlying primitive so that it has the desired value.

For example, in Figure 113-11, the RLOC = R1C1 constraint is attached to the instantiation (Inst1) of an example macro. It is added to the R0C0 value of the RLOC constraint on the flip-flop within the macro to obtain the new RLOC values. This functions the same for Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X macros except that the RLOC constraint uses XY designations.

For Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X, if the RLOC=X1Y1 constraint is attached to Inst1 of a macro, the X0Y0 value of the RLOC constraint on the flip-flop within the macro would be used to obtain the new RLOC values.

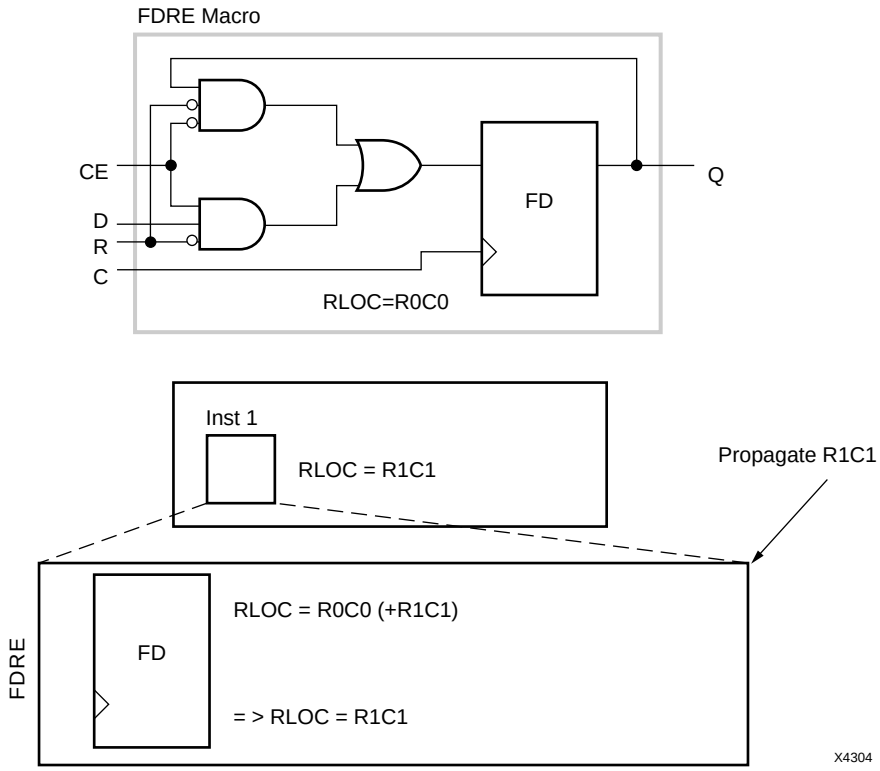


Figure 113-11: **Typical Use of a Xilinx Macro**

If you do not put an RLOC constraint on the flip-flop macro symbol, the underlying primitive symbol is the lone member of a set. The mapper removes RLOC constraints from a primitive that is the only member of a set or from a macro that has no RLOC objects below it.

LOC and RLOC Propagation through Design Flattening

NGDBuild continues to propagate LOC constraints down the design hierarchy. It adds this constraint to appropriate objects that are not members of a set. While RLOC constraint propagation is limited to sets, the LOC constraint is applied from its start point all the way down the hierarchy.

When the design is flattened, the row and column numbers of an RLOC constraint on an element are added to the row and column numbers of the RLOC constraints of the set members below it in the hierarchy. This feature gives you the ability to modify existing RLOC values in submodules and macros without changing the previously assigned RLOC values on the primitive symbols.

Specifying RLOC constraints to describe the spatial relationship of the set members to themselves allows the members of the set to float anywhere on the die as a unit. You can, however, fix the exact die location of the set members. The RLOC_ORIGIN constraint allows you to change the RLOC values into absolute LOC constraints that respect the structure of the set.

The design resolution program, NGDBuild, translates the RLOC_ORIGIN constraint into LOC constraints. The row and column values of the RLOC_ORIGIN are added individually to the members of the set after all RLOC modifications have been made to their row and column values by addition through the hierarchy. The final values are then turned into LOC constraints on individual primitives.

Fixing Members of a Set at Exact Die Locations

As noted in the previous section, you can fix the members of a set at exact die locations with the RLOC_ORIGIN constraint. You must use the RLOC_ORIGIN constraint with sets that include BUFT symbols. However, for sets that do not include BUFT symbols, you can limit the members of a set to a certain range on the die.

In this case, the set could “float” as a unit within the range until a final placement. Since every member of the set must fit within the range, it is important that you specify a range that defines an area large enough to respect the spatial structure of the set.

CLB-based Row/Column/Slice Designations

The syntax of this constraint is:

RLOC_RANGE=R*m1***C***n1***:R***m2***C***n2*

where the relative row numbers (*m1*, *m2*) and column numbers (*n1*, *n2*) can be non-zero positive numbers, or the wildcard (*) character.

This syntax allows for three kinds of range specifications as follows.

- R*r1*C*c1*:R*r2*C*c2*
  A rectangular region enclosed by rows *r1*, *r2*, and columns *c1*, *c2*
- R*C*c1*:R*C*c2*
  A region enclosed by the columns *c1* and *c2* (any row number)
- R*r1*C*:R*r2*C*
  A region enclosed by the rows *r1* and *r2* (any column number)

For the second and third kinds of specifications with wildcards, applying the wildcard character (*) differently on either side of the separator colon creates an error. For example, specifying R*C1:R2C* is an error since the wildcard asterisk is applied to rows on one side and to columns on the other side of the separator colon.

Slice-based XY Designations

The syntax of this constraint is the following:

RLOC_RANGE=X*m1***Y***n1***:X***m2***Y***n2*

where the relative X values (*m1*, *m2*) and Y values (*n1*, *n2*) can be non-zero positive numbers, or the wildcard (*) character.

This syntax allows for three kinds of range specifications:

- X*m1*Y*n1*:X*m2*Y*n2*
  A rectangular region bounded by the corners X*m1*Y*n1* and X*m2*Y*n2*
- X*Y*n1*:X*Y*m2*
  The region on the Y-axis between *n1* and *n2* (any X value)
- X*m1*Y*:X*m2*Y*
  A region on the X-axis between *m1* and *m2* (any Y value)

For the second and third kinds of specifications with wildcards, applying the wildcard character (*) differently on either side of the separator colon creates an error. For example,

specifying X*Y1:X2Y* is an error since the wildcard asterisk is applied to the X value on one side and to the Y value on the other side of the separator colon.

Specifying a Range

To specify a range, use the following syntax, which is equivalent to placing an RLOC_RANGE constraint on the schematic.

- For CLB-based Row / Column / Slice Designations:

  set_name **RLOC_RANGE=R***m1***C***n1***:R***m2***C***n2*

  The range identifies a rectangular area. You can substitute a wildcard (*) character for either the row number or the column number of both corners of the range.

- For Slice-based XY Designations:

  set_name **RLOC_RANGE=X***m1***Y***n1***:X***m2***Y***n2*

  The range identifies a rectangular area. You can substitute a wildcard (*) character for either the X value or the Y value of both corners of the range.

The bounding rectangle applies to all elements in a relationally placed macro, not just to the origin of the set.

The values of the RLOC_RANGE constraint are not simply added to the RLOC values of the elements. In fact, the RLOC_RANGE constraint does not change the values of the RLOC constraints on underlying elements. It is an additional constraint that is attached automatically by the mapper to every member of a set.

The RLOC_RANGE constraint is attached to design elements in exactly the same way as the RLOC_ORIGIN constraint. The values of the RLOC_RANGE constraint, like RLOC_ORIGIN values, must be non-zero positive numbers since they directly correspond to die locations.

If a particular RLOC set is constrained by an RLOC_ORIGIN or an RLOC_RANGE constraint in the design netlist and is also constrained in the UCF file, the UCF file constraint overrides the netlist constraint.

Toggling the Status of RLOC Constraints

Another important set modifier is the USE_RLOC constraint. It turns the RLOC constraints on and off for a specific element or section of a set. USE_RLOC can be either TRUE or FALSE.

The application of the USE_RLOC constraint is strictly based on hierarchy. A USE_RLOC constraint attached to an element applies to all its underlying elements that are members of the same set. If it is attached to a symbol that defines the start of a set, the constraint is applied to all the underlying member elements, which represent the entire set.

However, if it is applied to an element below the start of the set (for example, E in Figure 113-12), only the members of the set (H and I) below the specified element are affected. You can also attach the USE_RLOC constraint directly to a primitive symbol so that it affects only that symbol.

When the USE_RLOC=FALSE constraint is applied, the RLOC and set constraints are removed from the affected symbols in the NCD file. This process is different than that followed for the RLOC_ORIGIN constraint. For RLOC_ORIGIN, the mapper generates and outputs a LOC constraint in addition to all the set and RLOC constraints in the PCF file. The mapper does not retain the original constraints in the presence of a USE_RLOC=FALSE constraint because these cannot be turned on again in later programs.

Figure 113-12 illustrates the use of the USE_RLOC constraint to mask an entire set as well as portions of a set.

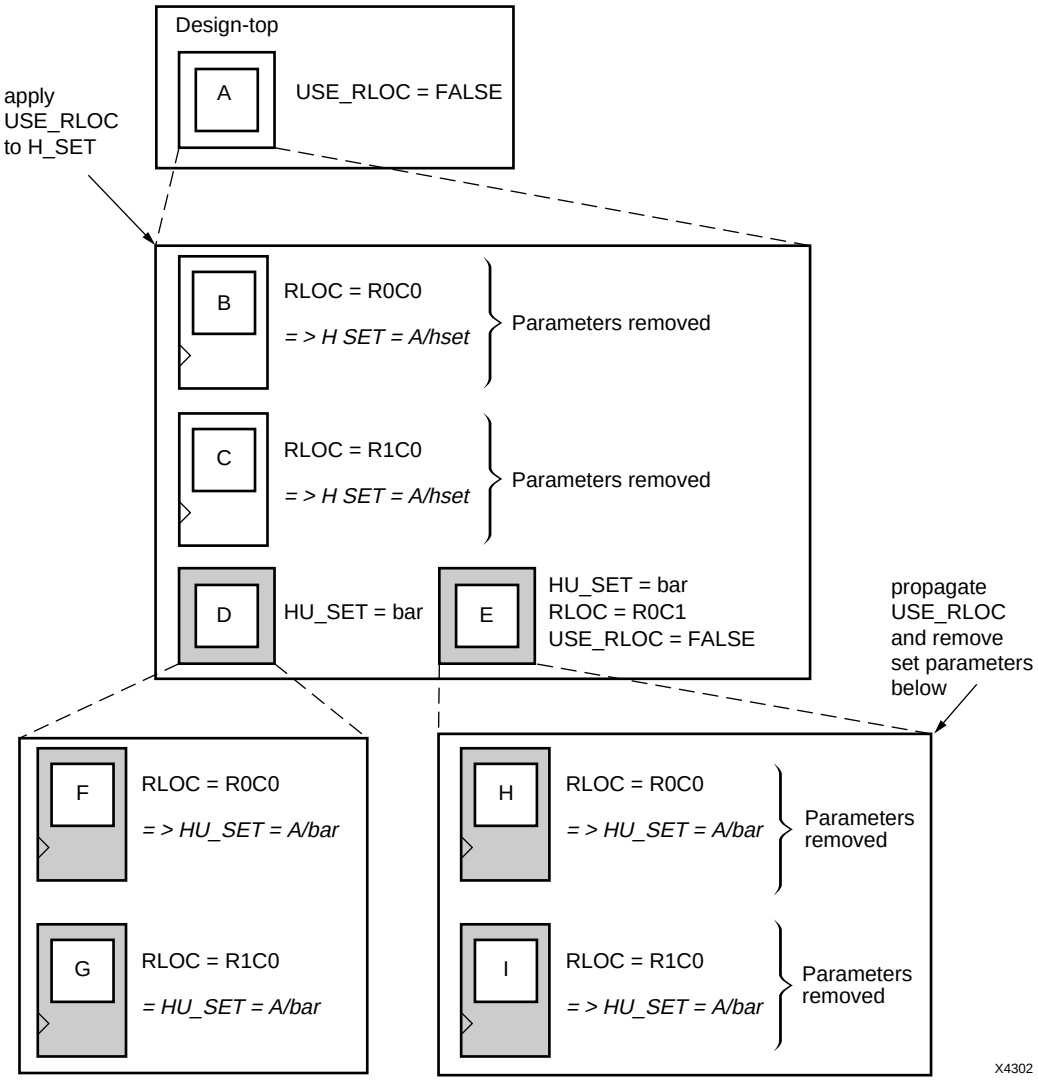


Figure 113-12: **Using the USE_RLOC Constraint to Control RLOC Application on H_SET and HU_SET Sets**

Applying the USE_RLOC constraint on U_SET sets is a special case because of the lack of hierarchy in the U_SET set. Because the USE_RLOC constraint propagates strictly in a hierarchical manner, the members of a U_SET set that are in different parts of the design hierarchy must be tagged separately with USE_RLOC constraints; no single USE_RLOC constraint is propagated to all the members of the set that lie in different parts of the hierarchy.

If you create a U_SET set through an instantiating macro, you can attach the USE_RLOC constraint to the instantiating macro to allow it to propagate hierarchically to all the members of the set.

You can create this instantiating macro by placing a U_SET constraint on a macro and letting the mapper propagate that constraint to every symbol with an RLOC constraint below it in the hierarchy.

Figure 113-13 illustrates an example of the use of the USE_RLOC=FALSE constraint. The USE_RLOC=FALSE on primitive E removes it from the U_SET set, and USE_RLOC=FALSE on element F propagates to primitive G and removes it from the U_SET set.

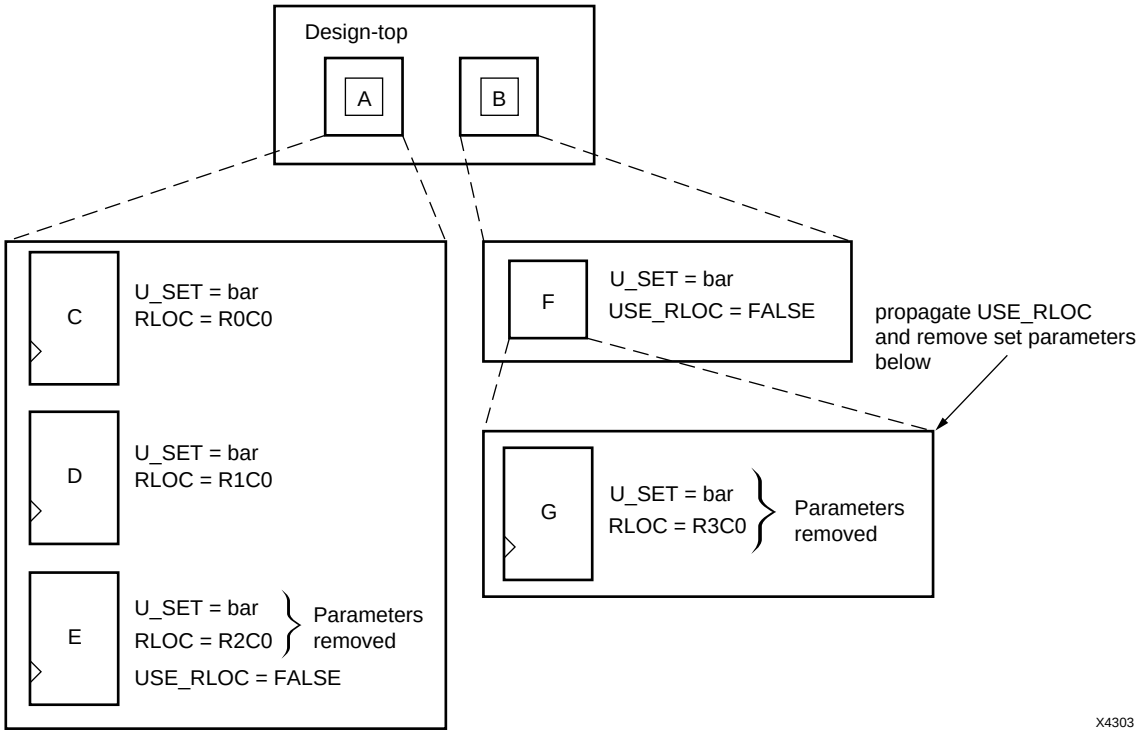


Figure 113-13: **Using the USE_RLOC Constraint to Control RLOC Application on U_SET Sets**

While propagating the USE_RLOC constraint, the mapper ignores underlying USE_RLOC constraints if it encounters elements higher in the hierarchy that already have USE_RLOC constraints. For example, if the mapper encounters an underlying element with a USE_RLOC=TRUE constraint during the propagation of a USE_RLOC=FALSE constraint, it ignores the newly encountered TRUE constraint.

Choosing an RLOC Origin when Using Hierarchy Sets

To specify a single origin for an RLOC set, use the following syntax, which is equivalent to placing an RLOC_ORIGIN constraint on the schematic.

- For CLB-based Row / Column / Slice Designations:

  set_name **RLOC_ORIGIN=R***m***C***n*

  where

  - *set_name* can be the name of any type of RLOC set — a U_SET, an HU_SET, or a system-generated H_SET
  - The origin itself is expressed as a row number and a column number representing the location of the elements at RLOC=R0C0

- For Slice-based XY Designations:

  set_name **RLOC_ORIGIN=X***m***Y***n*

  where

  - *set_name* can be the name of any type of RLOC set — a U_SET, an HU_SET, or a system-generated H_SET
  - The origin itself is expressed as an X and Y value representing the location of the elements at RLOC=X0Y0

When RLOC_ORIGIN is used in conjunction with an implicit H_SET (hierarchy set), it must be placed on the element that is the start of the H_SET set, that is, on the lowest common ancestor of all the members of the set.

If you apply RLOC_ORIGIN to an HU_SET constraint, place it on the element at the start of the HU_SET set, that is, on an element with the HU_SET constraint.

However, since there could be several elements linked together with the HU_SET constraint at the same node, the RLOC_ORIGIN constraint can be applied to only one of these elements to prevent more than one RLOC_ORIGIN constraint from being applied to the HU_SET set.

Similarly, when used with a U_SET constraint, the RLOC_ORIGIN constraint can be placed on only one element with the U_SET constraint. If you attach the RLOC_ORIGIN constraint to an element that has only an RLOC constraint, the membership of that element in any set is removed, and the element is considered the start of a new H_SET set with the specified RLOC_ORIGIN constraint attached to the newly created set.

In Figure 113-14, the elements B, C, D, F, and G are members of an H_SET set with the name A / h_set. This figure is the same as Figure 113-5 except for the presence of an RLOC_ORIGIN constraint at the start of the H_SET set (at A).

The RLOC_ORIGIN values are added to the resultant RLOC values at each of the member elements to obtain the values that are then converted by the mapper to LOC constraints. For example, the RLOC value of F, given by adding the RLOC value at E (R0C1) and that at F (R0C0), is added to the RLOC_ORIGIN value (R2C3) to obtain the value of (R2C4), which is then converted to a LOC constraint, LOC = CLB_R2C4.

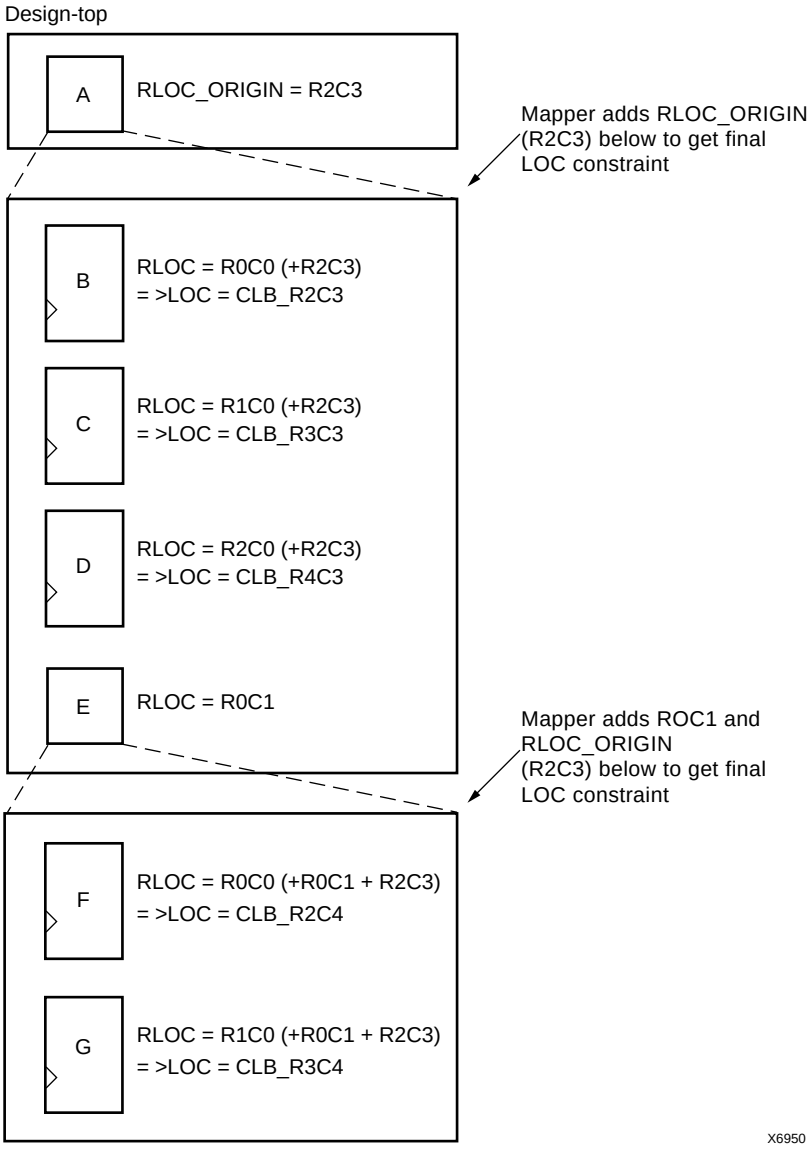


Figure 113-14: **Using an RLOC_ORIGIN Constraint to Modify an H_SET Set**

Figure 113-15 shows an example of an RLOC_ORIGIN constraint modifying an HU_SET constraint. The start of the HU_SET A / bar is given by element D or E. The RLOC_ORIGIN attached to E, therefore, applies to this HU_SET set. On the other hand, the RLOC_ORIGIN at A, which is the start of the H_SET set A / h_set, applies to elements B and C, which are members of the H_SET set.

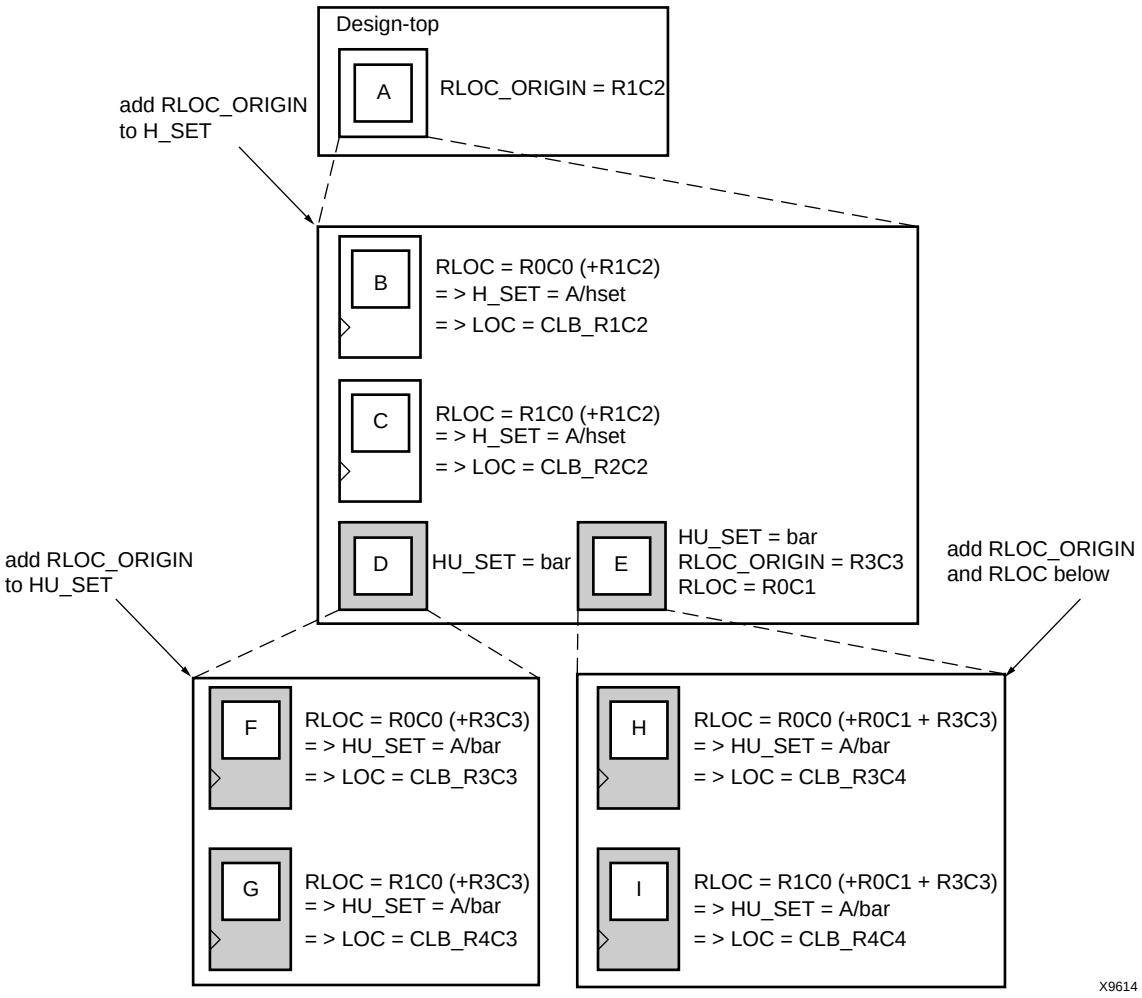


Figure 113-15: **Using an RLOC_ORIGIN to Modify H_SET and HU_SET Sets**

RLOC Examples

Schematic

Attach to an instance.

Attribute Name—RLOC

Attribute Values—See "RLOC Syntax".

VHDL

Before using RLOC, declare it with the following syntax:

```
attribute rloc: string;
```

After RLOC has been declared, specify the VHDL constraint as follows for Virtex, Virtex-E, Spartan-II, and Spartan-IIE:

```
attribute rloc of {component_name|entity_name|label_name}:
{component|entity|label} is "[element]RmCn[.extension]";
```

After RLOC has been declared, specify the VHDL constraint as follows for Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X, and Virtex-4:

```
attribute rloc of {component_name|entity_name|label_name}:
{component|entity|label} is "[element]XmYn[.extension]";
```

See "Guidelines for Specifying Relative Locations" for descriptions of valid values.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

The following code sample shows how to use RLOCs with a VHDL generate statement. The code is a simple example showing how to auto-generate the RLOCs for several instantiated FDEs. This methodology can be used with virtually any primitive.

```
LEN:for i in 0 to bits-1 generate
  constant row :natural:=((width-1)/2)-(i/2);
  constant column:natural:=0;
  constant slice:natural:=0;
  constant rloc_str : string := "R" & itoa(row) & "C" & itoa(column) &
".S" & itoa(slice);
  attribute RLOC of U1: label is rloc_str;
begin
  U1: FDE port map (
      Q  => dd(j),
      D  => ff_d,
      C  => clk,
      CE =>lcl_en(en_idx));
end generate LEN;
```

Verilog

Specify as follows for Virtex and Spartan-II:

```
// synthesis attribute rloc [of] {module_name|instance_name} [is]
[element]RmCn[.extension];
```

Specify as follows for Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4:

```
// synthesis attribute rloc [of] {module_name|instance_name} [is]
[element]XmYn[.extension];
```

See "Guidelines for Specifying Relative Locations" for descriptions of valid values.

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

- For Virtex, Virtex-E, Spartan-II, and Spartan-IIE, the following statement specifies that an instantiation of FF1 be placed in the CLB at row 4, column 4.

  ```
  INST "/Virtex/design/FF1" RLOC=R4C4;
  ```

- For Virtex, Virtex-E, Spartan-II, and Spartan-IIE, the following statement specifies that an instantiation of elemA be placed in the X flip-flop in the CLB at row 0, column 1.

  ```
  INST "/$1I87/elemA" RLOC=r0cl.S0;
  ```

- For Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4, the following statement specifies that an instantiation of FF1 be placed in a slice that is +4 X coordinates and +4 Y coordinates relative to the origin slice.

  ```
  INST “/V2/design/FF1” RLOC=X4Y4;
  ```

XCF

For Virtex, Virtex-E, Spartan-II, and Spartan-IIE:

```
BEGIN MODEL “entity_name”
 INST "instance_name" rloc=[element]RmCn[.extension];
END;
```

For Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4:

```
BEGIN MODEL “entity_name”
 INST "instance_name" rloc=[element]XmYn[.extension];
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

D rag logic to locations on the Floorplan view. To write out RLOCs, save the constraints to an NCF file via the Write RPM to NCF... command on the File pulldown menu. Refer to the “Write RPM to NCF Command” topic in the Floorplanner online help.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

RLOC_ORIGIN

RLOC_ORIGIN Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

RLOC_ORIGIN Applicable Elements

Instances or macros that are members of sets.

RLOC_ORIGIN Propagation Rules

RLOC_ORIGIN is a macro constraint and any attachment to a net is illegal.

RLOC_ORIGIN Description

RLOC_ORIGIN is a placement constraint. It fixes the members of a set at exact die locations. RLOC_ORIGIN must specify a single location, not a range or a list of several locations. For more information about RLOC_ORIGIN, see “Set Modifiers”.

RLOC_ORIGIN is required for a set that includes BUFT symbols. RLOC_ORIGIN cannot be attached to a BUFT instance.

RLOC_ORIGIN Syntax Examples

Schematic

Attach to an instance that is a member of a set.

Attribute Name—RLOC_ORIGIN

Attribute Values—See the UCF section.

VHDL

Before using RLOC_ORIGIN, declare it with the following syntax:

```
attribute rloc_origin: string;
```

After RLOC_ORIGIN has been declared, specify the VHDL constraint as follows:

```
attribute rloc_origin of {component_name|entity_name|label_name}:
{component|entity|label} is "value";
```

For Virtex, Virtex-E, Spartan-II, and Spartan-II E, *value* is **R***m***C***n*.

For Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X, *value* is **X***m***Y***n*.

See the UCF section for a description of valid values.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
// synthesis attribute rloc_origin [of] {module_name|instance_name}
[is] value;
```

For Virtex, Virtex-E, Spartan-II, and Spartan-IIE, *value* is **R***m***C***n*.

For Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X, *value* is **X***m***Y***n*.

See the UCF section for a description of valid values.

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

RLOC_ORIGIN Syntax for Architectures Using CLB-based Row/Column/Slice Specifications

```
RLOC_ORIGIN=RmCn
```

where *m* and *n* are positive or negative integers (including zero) representing relative row and column numbers, respectively.

The following statement specifies that any RLOC statement applied to FF1 uses the CLB at R4C4 as its reference point. For example, if RLOC=R0C2 for FF1, then the instantiation of FF1 is placed in the CLB that occupies row 4 (R0 + R4), column 6 (C2 + C4).

```
INST "/archive/designs/FF1" RLOC_ORIGIN=R4C4;
```

RLOC_ORIGIN Syntax for Architectures Using Slice-based XY Coordinates (Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X Only)

RLOC_ORIGIN=X*m*Y*n*

where *m* and *n* are positive or negative integers (including zero) representing relative X and Y coordinates, respectively.

The following statement specifies that an instantiation of FF1, which is a member of a set, be placed in the slice at X4Y4 relative to FF1. For example, if RLOC=X0Y2 for FF1, then the instantiation of FF1 is placed in the slice that is 0 rows to the right of X4 and 2 rows up from Y4 (X4Y6).

```
INST “/archive/designs/FF1” RLOC_ORIGIN=X4Y4;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

See the Write RPM to UCF Command section in the Floorplanner online help.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

RLOC_RANGE

RLOC_RANGE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

RLOC_RANGE Applicable Elements

Instances or macros that are members of sets.

RLOC_RANGE Description

RLOC_RANGE is a placement constraint. It is similar to RLOC_ORIGIN except that it limits the members of a set to a certain range on the die. The range or list of locations is meant to apply to all applicable elements with RLOCs, not just to the origin of the set.

RLOC_RANGE Propagation Rules

RLOC_RANGE is a macro constraint and any attachment to a net is illegal.

RLOC_RANGE Syntax Examples

Schematic

Attach to an instance that is a member of a set.

Attribute Name—RLOC_RANGE

Attribute Values—See the UCF section.

VHDL

Before using RLOC_RANGE, declare it with the following syntax:

```
attribute rloc_range: string;
```

After RLOC_RANGE has been declared, specify the VHDL constraint as follows:

```
attribute rloc_range of {component_name|entity_name|label_name}:
{component|entity|label} is "value";
```

For Virtex, Virtex-E, Spartan-II, and Spartan-IIE, *value* is **R***m1***C***n1*:**R***m2***C***n2*.

For Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X, *value* is **X***m1***Y***n1*:**X***m2***Y***n2*.

See the UCF section for a description of valid values.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
// synthesis attribute rloc_range [of] {module_name|instance_name}
[is] value;
```

For Virtex, Virtex-E, Spartan-II, and Spartan-IIE, *value* is **R***m1***C***n1*:**R***m2***C***n2*.

For Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X, *value* is **X***m1***Y***n1*:**X***m2***Y***n2*.

See the UCF section for a description of valid values.

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

For Architectures using CLB-based Row/Column/Slice Specifications

```
RLOC_RANGE=Rm1Cn1:Rm2Cn2
```

where the relative row numbers (*m1* and *m2*) and column numbers (*n1* and *n2*) can be positive integers (including zero) or the wildcard (*) character.

This syntax allows three kinds of range specifications, which are defined in "Set Modifiers".

The following statement specifies that an instantiation of the macro MACRO4 be placed within a region that is enclosed by the rows R4-R10 and the columns C4-C10.

```
INST "/archive/designs/MACRO4" RLOC_RANGE=R4C4:R10C10;
```

For Architectures using slice-based XY Specifications (Spartan-3, Virtex-II, Virtex-II Pro, and Virtex-II Pro X Only)

RLOC_RANGE=X*m1***Y***n1***:X***m2***Y***n2***

where the relative X values (*m1* and *m2*) and Y values (*n1* and *n2*) can be positive integers (including zero) or the wildcard (*) character.

This syntax allows three kinds of range specifications, which are defined in "Set Modifiers".

The following statement specifies that an instantiation of the macro MACRO4 be placed relative to other members of the set within a region that is bounded by X4Y4 in the lower left corner and by X10Y10 in the upper right corner.

```
INST "/archive/designs/MACRO4" RLOC_RANGE=X4Y4:X10Y10;
```

XCF

```
MODEL "entity_name" rloc_range=value;

BEGIN MODEL "entity_name"
 INST "instance_name" rloc_range=value;
END;
```

Constraints Editor

Not applicable.

PCF

RLOC_RANGE translates to a LOCATE constraint that has a range of sites. For example, **locate CLB_R1C1:CLB_R10C2**

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

ROM_EXTRACT

ROM_EXTRACT Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

ROM_EXTRACT Applicable Elements

You can apply ROM_EXTRACT globally or to a design element, or signal.

ROM_EXTRACT Description

ROM_EXTRACT is a synthesis constraint. The constraint enables or disables ROM macro inference. Allowed values are yes, and no (TRUE and FALSE ones are available in XCF as well). The default is **yes**. Typically, a ROM can be inferred from a Case statement where all assigned contexts are constant values.

ROM_EXTRACT Propagation Rules

Applies to the entity, module, or signal to which it is attached.

ROM_EXTRACT Syntax Examples

Schematic

Not applicable.

VHDL

Before using ROM_EXTRACT, declare it with the following syntax:

```
attribute rom_extract: string;
```

After ROM_EXTRACT has been declared, specify the VHDL constraint as follows:

```
attribute rom_extract of {signal_name|entity_name}: {signal|entity} is
“yes”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
 // synthesis attribute rom_extract [of] {module_name|signal_name} [is]
yes;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL “entity_name” rom_extract={yes|no|true|false};


BEGIN MODEL “entity_name”
 NET “signal_name” rom_extract={yes|no|true|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-rom_extract** command line option of the **run** command. Following is the basic syntax:

```
-rom_extract {YES|NO}
```

The default is **YES**.

Project Navigator

Set globally with the ROM Extraction option in the HDL Options tab of the Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

ROM_STYLE

ROM_STYLE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

ROM_STYLE Applicable Elements

You can apply ROM_STYLE globally or to an entity, module, or signal.

ROM_STYLE Description

ROM_STYLE is a synthesis constraint. It controls the way the macrogenerator implements the inferred ROM macros. ROM_EXTRACT must be set to YES to use ROM_STYLE. Allowed values are **AUTO**, **BLOCK** and **DISTRIBUTED**. The default value is **AUTO**, meaning that XST looks for the best implementation for each inferred ROM. The implementation style can be manually forced to use block ROM or distributed ROM resources available in the Virtex and Spartan-II series.

ROM_STYLE Propagation Rules

Applies to the entity, module, or signal to which it is attached.

ROM_STYLE Syntax Examples

Schematic

Not applicable.

VHDL

ROM_EXTRACT must be set to YES to use ROM_STYLE.

Before using ROM_STYLE, declare it with the following syntax:

```
attribute rom_style: string;
```

After ROM_STYLE has been declared, specify the VHDL constraint as follows:

```
attribute rom_style of {signal_name|entity_name}: {signal|entity} is
"{auto|block|distributed}";
```

The default value is **AUTO**.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

ROM_EXTRACT must be set to YES to use ROM_STYLE.

Specify as follows:

```
 // synthesis attribute rom_style [of] {module_name|signal_name} [is]
{auto|block|distributed};
```

The default value is **AUTO**.

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

ROM_EXTRACT must be set to YES to use ROM_STYLE.

```
MODEL "entity_name" rom_style={auto|block|distributed};

BEGIN MODEL "entity_name"
 NET "signal_name"  rom_style={auto|block|distributed};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

ROM_EXTRACT must be set to YES to use ROM_STYLE.

Define globally with the **-rom_style** command line option of the **run** command. Following is the basic syntax:

```
-rom_style {auto|distributed|block}
```

The default is **AUTO**.

Project Navigator

Not applicable.

SAFE_IMPLEMENTATION

SAFE_IMPLEMENTATION Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner II	Yes

SAFE_IMPLEMENTATION Applicable Elements

This constraint can be applied to an entire design via an XST command line, to a particular block (entity, architecture, component), and to a signal.

SAFE_IMPLEMENTATION Description

SAFE_IMPLEMENTATION is a synthesis constraint that allows you to implement State Machines in Safe mode. By implementing FSM in safe mode, XST collects all codes not participating in the normal FSM behavior and considers them as illegal. XST generates logic that returns FSM synchronously to the known state (reset state, power up state or state specified by the user via safe_recovery_state constraint).

Allowed values are YES and NO (TRUE and FALSE are available in XCF as well). By default, safe implementation is disabled (NO).

SAFE_IMPLEMENTATION Propagation Rules

Applies to an entity, component, module, or signal to which it is attached.

SAFE_IMPLEMENTATION Syntax Examples

Schematic

Not applicable.

VHDL

Before using SAFE_IMPLEMENTATION, declare it with the following syntax:

```
attribute safe_implementation: string;
```

After SAFE_IMPLEMENTATION has been declared, specify the VHDL constraint as follows:

```
attribute safe_implementation of
{entity_name|component_name|signal_name}: {entity|component|signal} is
"yes";
```

For a more detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute safe_implementation [of]
{module_name|signal_name} [is] “yes”;
```

For a more detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL “entity_name” safe_implementation={yes|no|true|false};
BEGIN MODEL “entity_name”
  NET “signal_name” safe_implementation={yes|no|true|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-safe_implementation** command line option of the **run** command. Following is the basic syntax:

```
-safe_implementation {YES|NO}
```

The default is **NO**.

Project Navigator

Set SAFE_IMPLEMENTATION globally with the Safe Implementation option in the HDL Options tab of the Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

SAFE_RECOVERY_STATE

SAFE_RECOVERY_STATE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner II	Yes

SAFE_RECOVERY_STATE Applicable Elements

This constraint can be applied to a signal representing state register.

SAFE_RECOVERY_STATE Description

SAFE_RECOVERY_STATE is a synthesis constraint that allows you to specify a particular recovery state when FSM is implemented in safe mode. By implementing FSM in safe mode, XST collects all codes not participating in the normal FSM behavior and considers them as illegal. XST generates logic that returns FSM synchronously to the known state (reset state, power up state or state specified by the user via safe_recovery_state constraint)

SAFE_RECOVERY_STATE Propagation Rules

Applies to a signal to which it is attached.

.

SAFE_RECOVERY_STATE Syntax Examples

Schematic

Not applicable.

VHDL

Before using SAFE_RECOVERY_STATE, declare it with the following syntax:

```
attribute safe_recovery_state: string;
```

After SAFE_RECOVERY_STATE has been declared, specify the VHDL constraint as follows:

```
attribute safe_recovery_state of {signal_name}:{signal} is "sl";
```

For a more detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
// synthesis attribute safe_recovery_state [of] {signal_name} [is] "sl"
```

For a more detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
BEGIN MODEL "entity_name"
  NET "signal_name" safe_recovery_state="s1";
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

SAVE NET FLAG

SAVE NET FLAG Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

SAVE NET FLAG Applicable Elements

Nets or signals

SAVE NET FLAG Description

SAVE NET FLAG is a basic mapping constraint. Attaching SAVE NET FLAG to nets or signals affects the mapping, placement, and routing of the design by preventing the removal of unconnected signals.

The flag prevents the removal of loadless or driverless signals. For loadless signals, the S constraint acts as a dummy OBUF load connected to the signal. For driverless signals the S constraint acts as a dummy IBUF driver connected to the signal.

If you do not have the S constraint on a net, any signal that cannot be observed or controlled via a path to an I/O primitive is removed.

The S constraint may prevent the trimming of logic connected to the signal.

Note: SAVE NET FLAG can be abbreviated S NET FLAG.

SAVE NET FLAG Propagation Rules

SAVE NET FLAG is a net or signal constraint. Any attachment to a design element is illegal.

SAVE NET FLAG prevents the removal of unconnected signals. If you do not have the S constraint on a net, any signal not connected to logic or an I/O primitive is removed.

SAVE NET FLAG Syntax Examples

Schematic

Attach to a net or signal.

Attribute Name—S

Attribute Values—TRUE, FALSE

VHDL

Before using SAVE, declare it with the following syntax:

```
attribute s: string;
```

After SAVE has been declared, specify the VHDL constraint as follows:

```
attribute s of signal_name: signal is “yes”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute s [of] signal_name [is] “yes”;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

The following statement specifies that the net or signal named $SIG_9 will not be removed.

```
NET “$SIG_9” S;
```

XCF

```
BEGIN MODEL “entity_name”
 NET  "signal_name" s=true;
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

SCHMITT_TRIGGER

SCHMITT_TRIGGER Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	No
Spartan-3E	No
Virtex-II	No
Virtex-II Pro	No
Virtex-II Pro X	No
Virtex-4	No
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	Yes

SCHMITT_TRIGGER Applicable Elements

Applies to all input pads and pad nets.

SCHMITT_TRIGGER Description

This constraint causes the attached input pad to be configured with Schmitt Trigger (hysteresis). This constraint applies to any input pad in the design.

SCHMITT_TRIGGER Propagation Rules

The constraint is a net or signal constraint. Any attachment to a macro, entity, or module is illegal.

SCHMITT_TRIGGER Syntax Examples

Schematic

Attach to a net

Attribute Name—SCHMITT_TRIGGER

Attribute Values—TRUE, FALSE

VHDL

Before using SCHMITT_TRIGGER, declare it with the following syntax:

```
attribute SCHMITT_TRIGGER: string;
```

After SCHMITT_TRIGGER has been declared, specify the VHDL constraint as follows:

```
attribute SCHMITT_TRIGGER of signal_name: signal is “true”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute SCHMITT_TRIGGER [of] signal_name [is] “true”;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

```
XILINX PROPERTY 'SCHMITT_TRIGGER mysignal';
```

UCF/NCF

```
NET “mysignal” SCHMITT_TRIGGER;
```

XCF

```
BEGIN MODEL “entity_name”
 NET  "signal_name" SCHMITT_TRIGGER=true;
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

XST Command Line

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

Project Navigator

Not applicable.

SHIFT_EXTRACT

SHIFT_EXTRACT Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

SHIFT_EXTRACT Applicable Elements

You can apply SHIFT_EXTRACT globally or to design elements and nets.

SHIFT_EXTRACT Description

SHIFT_EXTRACT is a synthesis constraint. It enables or disables logical shifter macro inference. Allowed values are **YES** (check box is checked) and **NO** (check box is not checked). (**TRUE** and **FALSE** ones are available in XCF as well). By default, logical shifter inference is enabled (**YES**).

SHIFT_EXTRACT Propagation Rules

Applies to the entity, module, or signal to which it is attached.

SHIFT_EXTRACT Syntax Examples

Schematic

Not applicable.

VHDL

Before using SHIFT_EXTRACT declare it with the following syntax:

```
attribute shift_extract: string;
```

After SHIFT_EXTRACT has been declared, specify the VHDL constraint as follows:

```
attribute shift_extract of {entity_name|signal_name}: {signal|entity}
is "yes";
```

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute shift_extract [of] {module_name|signal_name}
[is] "yes";
```

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL "entity_name" shift_extract={yes|no|true|false};


BEGIN MODEL "entity_name"
 NET "signal_name" shift_extract={yes|no|true|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-shift_extract** command line option of the **run** command. Following is the basic syntax:

```
-shift_extract {YES|NO}
```

The default is **YES**.

Project Navigator

Set SHIFT_EXTRACT globally with the Logical Shifter Extraction option in the HDL Options tab of the Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

SHREG_EXTRACT

SHREG_EXTRACT Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

SHREG_EXTRACT Applicable Elements

You can apply SHREG_EXTRACT globally or to design elements and signals.

SHREG_EXTRACT Description

SHREG_EXTRACT is a synthesis constraint. It enables or disables shift register macro inference. Allowed values are **YES** (check box is checked) and **NO** (check box is not checked). (**TRUE** and **FALSE** ones are available in XCF as well). By default, shift register inference is enabled.

SHREG_EXTRACT Propagation Rules

It applies to design elements or signals to which it is attached.

SHREG_EXTRACT Syntax Examples

Schematic

Not applicable.

VHDL

Before using SHREG_EXTRACT, declare it with the following syntax:

```
attribute shreg_extract : string;
```

After SHREG_EXTRACT has been declared, specify the VHDL constraint as follows:

```
attribute shreg_extract of {signal_name|entity_name}: {signal|entity}
is “yes”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
 // synthesis attribute shreg_extract [of] {module_name|signal_name}
[is] “yes”;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL “entity_name” shreg_extract={yes|no|true|false};


BEGIN MODEL “entity_name”
 NET “signal_name” shreg_extract={yes|no|true|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-shreg_extract** command line option of the **run** command. Following is the basic syntax:

```
-shreg_extract {YES|NO}
```

The default is **YES**.

Project Navigator

Set globally with the Shift Register Extraction option in the HDL Options tab of the Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

SIGNAL_ENCODING

SIGNAL_ENCODING Architecture Support

The following table indicates supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

SIGNAL_ENCODING Applicable Elements

SIGNAL_ENCODING can be applied globally or to a VHDL entity, Verilog module, or signal.

SIGNAL_ENCODING Description

SIGNAL_ENCODING is a synthesis constraint. This constraint selects the coding technique to use for internal signals. Available property values are auto, one-hot, and user. Selecting "one-hot" forces the encoding to a one-hot encoding, and "user" forces XST to keep the user's encoding. SIGNAL_ENCODING defaults to auto, meaning that the best coding technique is automatically selected for each individual signal.

SIGNAL_ENCODING Propagation Rules

Applies to the entity, module, or signal to which it is attached.

SIGNAL_ENCODING Syntax Examples

Schematic

Not applicable.

VHDL

Before using SIGNAL_ENCODING, declare it with the following syntax:

```
attribute SIGNAL_ENCODING: string;
```

After SIGNAL_ENCODING has been declared, specify the VHDL constraint as follows:

```
attribute SIGNAL_ENCODING of
{component_name|signal_name|entity_name|label_name}:
{component|signal|entity|label} is “{auto|one-hot|user}”;
```

The default is **auto**.

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
 // synthesis attribute SIGNAL_ENCODING [of]
{module_name|instance_name|signal_name} [is] {auto|one-hot|user};
```

The default is **auto**.

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL “entity_name” SIGNAL_ENCODING = {auto|one-hot|user};

BEGIN MODEL “entity_name”
 NET "net_name" SIGNAL_ENCODING = {auto|one-hot|user};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the -signal_encoding command line option of the run command. Following is the basic syntax: -signal_encoding {Auto | One-Hot | User}

The default is AUTO

Project Navigator

Not applicable.

SIM_COLLISION_CHECK

SIM_COLLISION_CHECK Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	No
Spartan-3E	No
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner II	No

SIM_COLLISION_CHECK Applicable Elements

Block RAM primitive elements

SIM_COLLISION_CHECK Description

This constraint is used to specify simulation model behavior when a read / write collision occurs on a memory location of Block RAM.

Allowed values: {AL, NONE, WARNING_ONLY, GENERATE_X_ONLY} If there is a read / write collision on a memory location in the V2 / V2P / V4 block RAM memory.

- WARNING_ONLY generates a WARNING message during simulation.

- GENERATE_X_ONLY generates X's on the outputs during simulation.

- ALL generates both a "WARNING message and X's on the output during simulation.

- NONE ignores collisions leading to unpredictable results during simulation.

SIM_COLLISION_CHECK Propagation Rules

It is illegal to attach SIM_COLLISION_CHECK to a net or signal.

SIM_COLLISION_CHECK Syntax Examples

Schematic

Attached to a block RAM primitive.

Attribute Name—SIM_COLLISION_CHECK

Attribute Values—WARNING_ONLY, GENERATE_X_ONLY, ALL, NONE

VHDL

Before using SIM_COLLISION_CHECK, declare it with the following syntax:

```
attribute sim_collision_check: string;
```

After SIM_COLLISION_CHECK has been declared, specify the VHDL constraint as follows:

```
attribute sim_collision_check of {component_name|label_name}:
{component|label} is “sim_collision_check_value”;
```

See the UCF section for a description of the sim_collision_check values.

Verilog

Specify as follows:

```
 // synthesis attribute sim_collision_check [of]
{module_name}|instance_name} [is] “sim_collision_check_value”;
```

See the UCF / NCF section for a description of the B_INPUT values.

For a more detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

Not applicable.

UCF

The following statement set the SIM_COLLISION_CHECK constraint for an instantiation of an I / O primitive element y2.

```
INST “$1187/y2 SIM_COLLISION_CHECK={WARNING_ONLY, GENERATE_X_ONLY,
ALL, NONE);
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

SLEW

SLEW Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

SLEW Applicable Elements

Output primitives, output pads, bidirectional pads

You can also attach SLEW to the net connected to the pad component in a UCF file. NGDBuild transfers SLEW from the net to the pad instance in the NGD file so that it can be processed by the mapper. Use the following syntax:

```
NET "net_name" slew={FAST|SLOW};
```

SLEW Description

SLEW has two possible arguments: FAST or SLOW.

FAST increases the speed of an IOB output. FAST produces a faster output but may increase noise and power consumption. See "FAST" for details.

SLOW stipulates that the slew rate limited control should be enabled. See "SLOW".

SLEW Propagation Rules

SLEW is illegal when attached to a net except when the net is connected to a pad. In this case, SLEW is treated as attached to the pad instance.

When attached to a design element, SLEW propagates to all applicable elements in the hierarchy within the design element.

SLEW Syntax Examples

Schematic

Attach to a valid instance.

Attribute Name—SLEW

Attribute Values—FAST, SLOW

VHDL

Before using SLEW, declare it with the following syntax:

```
attribute slew : string;
```

After SLEW has been declared, specify the VHDL constraint as follows:

```
attribute slew of {entity_name|signal_name}: {entity|signal} is
"{FAST|SLOW}";
```

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify SLEW as follows:

```
// synthesis attribute slew [of] object_list [is] {FAST|SLOW}
```

where *object_list* is a comma separated list of specific names of modules and signals.

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

The following statement establishes a slew rate for an instantiation of the element y2.

```
INST "$1I87/y2" SLEW={FAST|SLOW};
```

The following statement establishes a slew rate for the pad to which net1 is connected.

```
NET "net1" SLEW={FAST|SLOW};
```

XCF

```
MODEL “entity_name” slew={FAST|SLOW};

BEGIN MODEL “entity_name”
 NET  "signal_name" slew={FAST|SLOW};
END;
```

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

You can select a SLEW rate (FAST or SLOW) for any output pad signal in the Ports tab (I/O Configuration Options).

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

SLICE_PACKING

SLICE_PACKING Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

SLICE_PACKING Applicable Elements

Global

SLICE_PACKING Description

This synthesis option enables the XST internal packer. The packer attempts to pack critical LUT-to-LUT connections within a slice or a CLB. This exploits the fast feedback connections among the LUTs in a CLB.

SLICE_PACKING Propagation Rules

Not applicable.

SLICE_PACKING Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-slice_packing** command line option of the **run** command. Following is the basic syntax:

```
-slice_packing {yes|no}
```

The default is Yes.

Project Navigator

Set globally with the Slice Packing option in the Xilinx Specific Options tab in the Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

SLICE_UTILIZATION_RATIO

SLICE_UTILIZATION_RATIO Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

SLICE_UTILIZATION_RATIO Applicable Elements

SLICE_UTILIZATION_RATIO can be applied globally or to a VHDL entity or Verilog module.

SLICE_UTILIZATION_RATIO Description

SLICE_UTILIZATION_RATIO is an area constraint that defines the area size (in %) that XST must not exceed during timing optimization.

If the area constraint cannot be satisfied, XST will make timing optimization regardless of the area constraint.

Please refer to "Speed Optimization Under Area Constraint" section in the *XST User Guide* for more information.

SLICE_UTILIZATION_RATIO Propagation Rules

Applies to the entity or module to which it is attached.

SLICE_UTILIZATION_RATIO Syntax Examples

Schematic

Not applicable.

VHDL

Before using SLICE_UTILIZATION_RATIO, declare it with the following syntax:

```
attribute slice_utilization_ratio: string;
```

After SLICE_UTILIZATION_RATIO has been declared, specify the VHDL constraint as follows:

```
attribute slice_utilization_ratio of entity_name : entity is "integer";
```

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
// synthesis attribute slice_utilization_ratio [of] module_name} [is]
integer;
```

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

XCF

```
MODEL "entity_name" slice_utilization_ratio=integer;
```

Integer range is 0 to 100.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-slice_utilization_ratio** command line option of the **run** command. Following is the basic syntax:

```
-slice_utilization_ratio integer
```

The integer range is 0 to 100.

Project Navigator

Set globally with the Slice Utilization Ratio option in the Synthesis Options tab of the Process Properties dialog box in the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

SLICE_UTILIZATION_RATIO_MAXMARGIN

SLICE_UTILIZATION_RATIO_MAXMARGIN Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

SLICE_UTILIZATION_RATIO_MAXMARGIN Applicable Elements

SLICE_UTILIZATION_RATIO_MAXMARGIN can be applied globally or to a VHDL entity or Verilog module.

SLICE_UTILIZATION_RATIO_MAXMARGIN Description

SLICE_UTILIZATION_RATIO_MAXMARGIN is closely related to SLICE_UTILIZATION_RATIO.

It defines the margin (in %) in which XST may consider that the area constraint is satisfied and timing optimization can be continued. Please refer to "Speed Optimization Under Area Constraint" section in *XST User Guide* for more information.

SLICE_UTILIZATION_RATIO_MAXMARGIN Propagation Rules

Applies to the entity or module to which it is attached.

SLICE_UTILIZATION_RATIO_MAXMARGIN Syntax Examples

Schematic

Not applicable.

VHDL

Before using SLICE_UTILIZATION_RATIO_MAXMARGIN, declare it with the following syntax:

```
attribute slice_utilization_ratio_maxmargin: string;
```

After SLICE_UTILIZATION_RATIO_MAXMARGIN has been declared, specify the VHDL constraint as follows:

```
attribute slice_utilization_ratio_maxmargin of entity_name : entity is
"integer";
```

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
// synthesis attribute slice_utilization_ratio_maxmargin [of]
module_name [is] integer;
```

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

XCF

```
MODEL "entity_name" slice_utilization_ratio_maxmargin=integer;
```

Integer range is 0 to 100.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-slice_utilization_ratio_maxmargin** command line option of the **run** command. Following is the basic syntax:

```
-slice_utilization_ratio_maxmargin integer
```

The integer range is 0 to 100.

Project Navigator

Not applicable.

SLOW

SLOW Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	No
Spartan-3E	No
Virtex-II	No
Virtex-II Pro	No
Virtex-II Pro X	No
Virtex-4	No
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

SLOW Applicable Elements

Output primitives, output pads, bidirectional pads

You can also attach SLOW to the net connected to the pad component in a UCF file. NGDBuild transfers SLOW from the net to the pad instance in the NGD file so that it can be processed by the mapper. Use the following UCF syntax:

```
NET "net_name" SLOW;
```

SLOW Description

SLOW is a basic fitter constraint. It stipulates that the slew rate limited control should be enabled.

SLOW Propagation Rules

SLOW is illegal when attached to a net except when the net is connected to a pad. In this case, SLOW is treated as attached to the pad instance.

When attached to a design element, SLOW propagates to all applicable elements in the hierarchy within the design element.

SLOW Syntax Examples

Schematic

Attach to a valid instance.

Attribute Name—SLOW

Attribute Values—TRUE, FALSE

VHDL

Before using SLOW, declare it with the following syntax:

```
attribute slow : string
```

After SLOW has been declared, specify the VHDL constraint as follows:

```
attribute slow of {signal_name|entity_name}: {signal|entity} is “true”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
 // synthesis attribute slow [of] {module_name|signal_name} [is]
“true”;
```

For a detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

```
XILINX PROPERTY 'SLOW mysignal';
```

UCF/NCF

The following statement establishes a slow slew rate for an instantiation of the element y2.

```
INST “$1I87/y2” SLOW;
```

The following statement establishes a slow slew rate for the pad to which net1 is connected.

```
NET “net1” SLOW;
```

XCF

Not applicable.

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

In the Ports tab grid with I/O Configuration Options checked, click the FAST/SLOW column in the row with the desired output port name and choose SLOW from the drop down list.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

SRVAL

SRVAL Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

SRVAL Applicable Elements

RAMB16_Sn (single-port block RAM)

SRVAL Description

SRVAL is a basic initialization constraint. In Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4, each bit in the output register can be initialized upon assertion of the SSR input to either a 0 or a 1. SRVAL defines the state of the output register for a single-port RAMB16 that results from assertion of its SSR (set/reset) input. The SRVAL property sets the output register value independently of the INIT value.

SRVAL Propagation Rules

It is illegal to attach SRVAL to a net.

When attached to a design element, SRVAL propagates to all applicable elements in the hierarchy within the design element.

SRVAL Syntax Examples

Schematic

Attach to a logic symbol.

Attribute Name—SRVAL

Attribute Values—*value*

See the UCF section for a discussion of *value*.

VHDL

Before using SRVAL, declare it with the following syntax:

```
attribute srval: string;
```

After SRVAL has been declared, specify the VHDL constraint as follows:

```
attribute srval of {component_name|entity_name|label_name}:
{component|entity|label} is "value";
```

See the UCF section for a description of *value*.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute srval [of] {module_name|instance_name} [is]
value;
```

See the UCF section for a description of *value*.

For a detailed discussion of the basic Verilog syntax, see "Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name" SRVAL=value;
```

where *value* is a hexadecimal number that represents the output register value upon assertion of the SSR input, depending on the width of the RAMB16 port. For every 4-bits, one hexadecimal value (0 through F) can be entered.

For those ports that include parity bits, the SRVAL value specifies the parity portion of the output register in the high order bit position, followed by the data portion. For example, to initialize data to zero and parity to one, you would set SRVAL to "100" for a 9-bit port, to "30000" for an 18-bit port, and to "F00000000" for a 36-bit port.

If the SRVAL constraint is not specified, the RAMB16 output register is set to zeros upon assertion of the SSR input.

The following statement specifies that the 9-bits of the output register of an RAMB16_S9 be set to 100 upon assertion of its SSR input.

```
INST “foo/bar” SRVAL=100;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

SRVAL_A

SRVAL_A Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

SRVAL_A Applicable Elements

Port A of RAMB16_Sm_Sn(dual-port block RAM)

SRVAL_A Description

SRVAL_A is a basic initialization constraint. In Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4, each bit in a RAMB16's output register can be initialized to either a 0 or a 1 upon assertion of its set/reset input. SRVAL_A initializes the port A (Sm) output register for dual-port RAMB16 components upon assertion of the SSRA input. SRVAL_A sets the value for port A independently of the INIT_A value.

SRVAL_A Propagation Rules

It is illegal to attach SRVAL_A to a net or signal.

When attached to a design element, SRVAL_A propagates to all applicable elements in the hierarchy within the design element.

SRVAL_A Syntax Examples

Schematic

Attach to a logic symbol.

Attribute Name—SRVAL_A

Attribute Values—*value*

See the UCF section for a discussion of *value*.

VHDL

Before using SRVAL_A, declare it with the following syntax:

```
attribute srval_a: string;
```

After SRVAL_A has been declared, specify the VHDL constraint as follows:

```
attribute srval_a of {component_name|entity_name|label_name}:
{compound|entity|label} is "value";
```

See the UCF section for a description of *value*.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
// synthesis attribute srval_a [of] {module_name|instance_name} [is]
value;
```

See the UCF section for a description of *value*.

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name" SRVAL_A=value;
```

where *value* is a hexadecimal number that defines the initialization string for the output register, depending on the width of port A. For every 4-bits, one hexadecimal value (0 through F) can be entered.

For those ports that include parity bits, the SRVAL_A value specifies the parity portion of the output register in the high order bit position, followed by the data portion. For example, to initialize data to zero and parity to one, you would set SRVAL_A to "100" for a 9-bit port, to "30000" for an 18-bit port, and to "F00000000" for a 36-bit port.

If SRVAL_A is not specified, the port A output register is initialized with zeros upon assertion of the SSRA input.

The following statement specifies that the 2 bits of the port A output register of an RAMB16_S2_S9 be set to 100 upon assertion of the SSRA input.

```
INST “foo/bar” SRVAL_A=100;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

SRVAL_B

SRVAL_B Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

SRVAL_B Applicable Elements

Port B of RAMB16_Sm_Sn (dual-port block RAM)

SRVAL_B Description

SRVAL_B is a basic initialization constraint. In Spartan-3, Virtex-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4, each bit in a RAMB16's output register can be initialized to either a 0 or a 1 upon assertion of its set / reset input. SRVAL_B initializes the port B (Sn) output register for dual-port RAMB16 components upon assertion of the SSRB input. SRVAL_B sets the value for port B independent of the INIT_B value.

SRVAL_B Propagation Rules

It is illegal to attach SRVAL_B to a net or signal.

When attached to a design element, SRVAL_B propagates to all applicable elements in the hierarchy within the design element.

SRVAL_B Syntax Examples

Schematic

Attach to a logic symbol.

Attribute Name—SRVAL_B

Attribute Values—*value*

See the UCF section for a discussion of *value*.

VHDL

Before using SRVAL_B, declare it with the following syntax:

```
attribute srval_b: string;
```

After SRVAL_B has been declared, specify the VHDL constraint as follows:

```
attribute srval_b of {component_name|entity_name|label_name}:
{component|entity|label} is "value";
```

See the UCF section for a description of *value*.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute srval_b [of] {module_name|instance_name} [is]
value;
```

See the UCF section for a description of *value*.

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name" SRVAL_B=value;
```

where *value* is a hexadecimal number that defines the initialization string for the output register, depending on the width of port B. For every 4-bits, one hexadecimal value (0 through F) can be entered.

For those ports that include parity bits, the SRVAL_B value specifies the parity portion of the output register in the high order bit position, followed by the data portion. For example, to initialize data to zero and parity to one, you would set SRVAL_B to "100" for a 9-bit port, to "30000" for an 18-bit port, and to "F00000000" for a 36-bit port.

If the SRVAL_B constraint is not specified, the port B output register is initialized with zeros upon assertion of the SSRB input.

The following statement specifies that the 9 bits of the port B output register of an RAMB16_S2_S9 be set to 100 upon assertion of the SSRB input.

```
INST “foo/bar” SRVAL_B=100;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

STARTUP_WAIT

STARTUP_WAIT Architecture Support

The numbers in the second column indicate applicable elements. See the next section.

Architecture	Supported/Unsupported
Virtex	1
Virtex-E	1, 2
Spartan-II	1, 2
Spartan-IIE	1, 2
Spartan-3	1, 2
Spartan-3E	1, 2
Virtex-II	1, 2
Virtex-II Pro	1, 2
Virtex-II Pro X	1, 2
Virtex-4	1, 2
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

STARTUP_WAIT Applicable Elements

1. CLKDLL, CLKDLLE (Virtex-E only), CLKDLLHF, or BUFGDLL instance

2. DCM instance

STARTUP_WAIT Description

STARTUP_WAIT is a basic DLL / DCM constraint. For Spartan-II, Spartan-IIE, Spartan-3, Virtex, Virtex-II, Virtex-II Pro, Virtex-II Pro X, Virtex-E devices, and Virtex-4, STARTUP_WAIT controls whether the DONE signal (device configuration) can go High (indicating that the device is fully configured). In conjunction with this setting this constraint, the FPGA startup sequence must also be modified to insert a LCK cycle before the cycle that is to be postponed (either the DONE cycle or GWE cycle are typical choices).

For all primitives, setting this to be TRUE means that the DONE signal will not go High until the LOCKED signal goes HIGH for the DLL or DCM that has STARTUP_WAIT set. STARTUP_WAIT will in no way prevent LOCKED from going High.

STARTUP_WAIT Propagation Rules

It is illegal to attach STARTUP_WAIT to a net or signal.

When attached to a design DLL / DCM, STARTUP_WAIT propagates to all applicable elements of the DLL / DCM.

STARTUP_WAIT Syntax Examples

Schematic

Attach to a valid instance.

Attribute Name—STARTUP_WAIT

Attribute Values—TRUE, FALSE

VHDL

Before using STARTUP_WAIT, declare it with the following syntax:

```
attribute startup_wait: string;
```

After STARTUP_WAIT has been declared, specify the VHDL constraint as follows:

```
attribute startup_wait of {component_name|label_name}:
{component|label} is “true”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
 // synthesis attribute startup_wait [of] {module_name|instance_name}
[is] “true”;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST “instance_name” STARTUP_WAIT={TRUE|FALSE};
```

where

- TRUE specifies that the DONE signal cannot go High until the instance assigned this property locks.
- FALSE, the default, specifies that the locking of the instance has no impact on the DONE signal or the Spartan-3, Virtex-II, Virtex-II Pro, or Virtex-II Pro X LOCKED signal.

The following statement specifies that the DONE signal cannot go High until the foo / bar instance locks.

```
INST “foo/bar” STARTUP_WAIT=TRUE;
```

XCF

```
BEGIN MODEL “entity_name”
 INST "instance_name" STARTUP_WAIT ={true|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

SYSTEM_JITTER

SYSTEM_JITTER Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	No
Spartan-3E	No
Virtex-II	No
Virtex-II Pro	No
Virtex-II Pro X	No
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

SYSTEM_JITTER Applicable Elements

Applies globally to the entire design.

SYSTEM_JITTER Description

This constraint specifies the system jitter of the design. System jitter depends on various design conditions -- for example, the number of flip-flops changing at one time and the number of I/Os changing. SYSTEM_JITTER applies to all of the clocks within a design. It will be combined with the INPUT_JITTER keyword on the PERIOD constraint to generate the Clock Uncertainty value that is shown in the timing report.

SYSTEM_JITTER Propagation Rules

Not applicable.

SYSTEM_JITTER Syntax Examples

Schematic

Attach to a valid instance.

Attribute Name—SYSTEM_JITTER

VHDL

Before using SYSTEM_JITTER, declare it with the following syntax:

```
attribute SYSTEM_JITTER: string;
```

After SYSTEM_JITTER has been declared, specify the VHDL constraint as follows:

```
attribute SYSTEM_JITTER of
{component_name|signal_name|entity_name|label_name}:
{component|signal|entity|label} is "value ns";
```

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute SYSTEM_JITTER [of]
{module_name|instance_name|signal_name} [is] value ns;
```

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
SYSTEM_JITTER= value ns;
```

where *value* is a numerical value. The default is ns.

For Virtex-II, Virtex-II Pro, and Virtex-II Pro X, the default is 0.

XCF

```
MODEL "entity_name" SYSTEM_JITTER = value ns;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

TEMPERATURE

TEMPERATURE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

Availability depends on the release of characterization data.

TEMPERATURE Applicable Elements

Global

TEMPERATURE Description

TEMPERATURE is an advanced timing constraint. It allows the specification of the operating junction temperature. TEMPERATURE provides a means of prorating device delay characteristics based on the specified temperature. Prorating is a scaling operation on existing speed file delays and is applied globally to all delays.

Each architecture has its own specific range of valid operating temperatures. If the entered temperature does not fall within the supported range, TEMPERATURE is ignored and an architecture-specific worst-case value is used instead. Also note that the error message for this condition does not appear until static timing.

TEMPERATURE Propagation Rules

It is illegal to attach TEMPERATURE to a net.

TEMPERATURE Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

```
TEMPERATURE=value [C |F| K];
```

where

- *value* is a real number specifying the temperature
- C, K, and F are the temperature units
  - F is degrees Fahrenheit
  - K is degrees Kelvin
  - C is degrees Celsius, the default

The following statement specifies that the analysis for everything relating to speed file delays assumes a junction temperature of 25 degrees Celsius.

```
TEMPERATURE=25 C;
```

XCF

Not yet supported.

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

In the Misc tab, click Specify next to Temperature and fill out the temperature dialog box.

PCF

The same as UCF.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

TIG

TIG Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

TIG Applicable Elements

Nets, pins, instances

TIG Description

TIG (Timing IGnore) is a basic timing constraint and a synthesis constraint. It causes paths that fan forward from the point of application (of TIG) to be treated as if they do not exist (for the purposes of the timing model) during implementation.

You may apply a TIG relative to a specific timing specification.

The value of TIG may be any of the following:

- Empty (global TIG that blocks all paths)
- A single TSid to block
- A comma separated list of TSids to block, for example

```
NET “RESET” TIG=TS_fast, TS_even_faster;
```

XST fully supports TIG constraint except the case, where TIG is used with FROM_TO constraint.

TIG Propagation Rules

If TIG is attached to a net, primitive pin, or macro pin, all paths that fan forward from the point of application of the constraint are treated as if they do not exist for the purposes of timing analysis during implementation. In the following figure, NET C is ignored. However, note that the lower path of NET B that runs through the two OR gates would not be ignored.

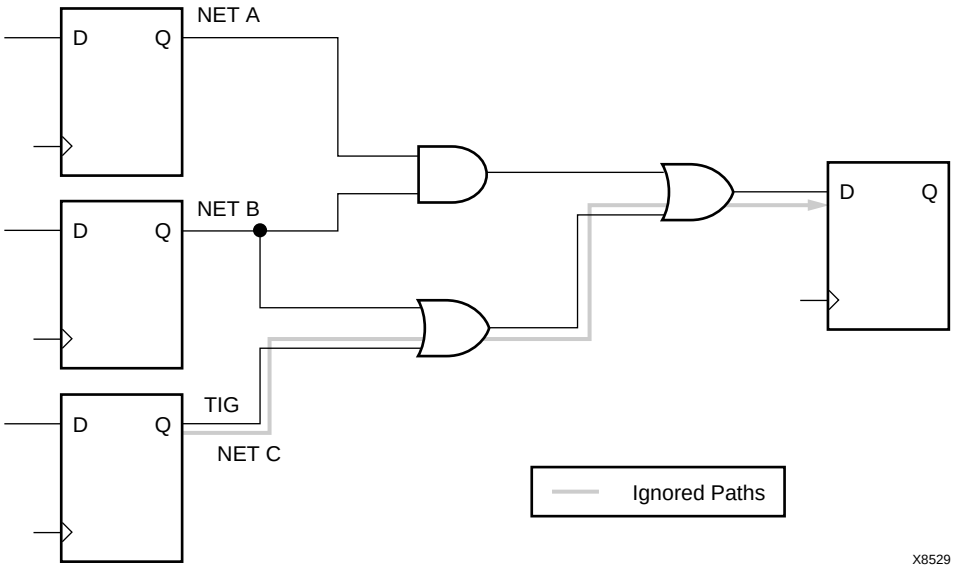


Figure 137-1: **TIG Example**

The following constraint would be attached to a net to inform the timing analysis tools that it should ignore paths through the net for specification TS43:

Schematic syntax

```
TIG = TS43
```

UCF syntax

```
NET “net_name” TIG = TS43;
```

You cannot perform path analysis in the presence of combinatorial loops. Therefore, the timing tools ignore certain connections to break combinatorial loops. You can use the TIG constraint to direct the timing tools to ignore specified nets or load pins, consequently controlling how loops are broken.

TIG Syntax Examples

Schematic

Attach to a net or pin.

Attribute Name—TIG

Attribute Values—*value*

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
NET "net_name" TIG;
PIN "ff_inst.RST" TIG=TS_1;
INST "instance_name" TIG=TS_2;
TIG=TSidentifier1,..., TSidentifiern
```

where *identifier* refers to a timing specification that should be ignored.

When attached to an instance, TIG is pushed to the output pins of that instance. When attached to a net, TIG pushes to the drive pin of the net. When attached to a pin, TIG applies to the pin.

The following statement specifies that the timing specifications TS_fast and TS_even_faster will be ignored on all paths fanning forward from the net RESET.

```
NET "RESET" TIG=TS_fast, TS_even_faster;
```

XCF

Same as the UCF syntax.

XST fully supports TIG constraint except the case, where TIG is used with FROM_TO constraint. TIG can be applied to the nets, situated in the CORE files (EDIF, NGC) as well.

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

In the Advanced tab, click Specify next to "False Paths (FROM TO TIG)" and fill out the FROM / THRU / TO dialog box or click Specify next to "False Paths by Net (NET TIG)" and fill out the Timing Ignore dialog box.

PCF

item **TIG;**

item **TIG = ;**

item **TIG = TS***identifier***;**

where *item* is:

- **PIN** *name*
- **PATH** *name*
- *path specification*
- **NET** *name*
- **TIMEGRP** *name*
- **BEL** *name*
- **COMP** *name*
- **MACRO** *name*

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

TIMEGRP

TIMEGRP Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

TIMEGRP Applicable Elements

Design elements or nets

TIMEGRP Description

TIMEGRP is a basic grouping constraint. In addition to naming groups using the TNM identifier, you can also define groups in terms of other groups. You can create a group that is a combination of existing groups by defining a TIMEGRP constraint.

You can place TIMEGRP constraints in a constraints file (UCF or NCF).

You can use TIMEGRP attributes to create groups using the following methods.

- Combining multiple groups into one
- Creating groups by exclusion
- Defining flip-flop subgroups by clock sense

The following subsections discuss each method in detail.

Combining Multiple Groups into One

You can define a group by combining other groups. The following syntax example illustrates the simple combining of two groups:

UCF syntax

```
TIMEGRP "big_group"="small_group" "medium_group";
```

In this syntax example, *small_group* and *medium_group* are existing groups defined using a TNM or TIMEGRP attribute.

A circular definition, as shown below, causes an error when you run your design through NGDBuild:

UCF syntax:

```
TIMEGRP "many_ffs"="ffs1" "ffs2";
TIMEGRP "ffs1"="many_ffs" "ffs3";
```

Creating Groups by Exclusion

You can define a group that includes all elements of one group except the elements that belong to another group, as illustrated by the following syntax examples:

UCF syntax

```
TIMEGRP "group1"="group2" EXCEPT "group3";
```

where

- *group1* represents the group being defined. It contains all of the elements in *group2* except those that are also in *group3*.
- *group2* and *group3* can be a valid TNM, predefined group, or TIMEGRP attribute.

As illustrated by the following example, you can specify multiple groups to include or exclude when creating the new group.

UCF syntax

```
TIMEGRP "group1"="group2" "group3" EXCEPT "group4" "group5";
```

The example defines a *group1* that includes the members of *group2* and *group3*, except for those members that are part of *group4* or *group5*. All of the groups before the keyword EXCEPT are included, and all of the groups after the keyword are excluded.

Defining Flip-Flop Subgroups by Clock Sense

You can create subgroups using the keywords RISING and FALLING to group flip-flops triggered by rising and falling edges.

UCF syntax

```
TIMEGRP "group1"=RISING ffs;
TIMEGRP "group2"=RISING "ffs_group";
TIMEGRP "group3"=FALLING ffs;
TIMEGRP "group4"=FALLING "ffs_group";
```

group1 to *group4* are new groups being defined. The *ffs_group* must be a group that includes only flip-flops.

Keywords, such as EXCEPT, RISING, and FALLING, appear in the documentation in upper case; however, you can enter them in either lower or upper case. You cannot enter them in a combination of lower and upper case.

The following example defines a group of flip-flops that switch on the falling edge of the clock.

UCF syntax:

```
TIMEGRP “falling_ffs”=FALLING ffs;
```

Defining Latch Subgroups by Gate Sense

Groups of type LATCHES (no matter how these groups are defined) can be easily separated into transparent high and transparent low subgroups. The TRANSHI and TRANSLO keywords are provided for this purpose and are used in TIMEGRP statements like the RISING and FALLING keywords for flip-flop groups.

UCF syntax:

```
TIMEGRP “lowgroup”=TRANSLO “latchgroup”;
TIMEGRP “highgroup”=TRANSHI “latchgroup”;
```

Creating Groups by Pattern Matching

When creating groups, you can use wildcard characters to define groups of symbols whose associated net names match a specific pattern. This is typically used in schematic designs where net names are specified, not instance names. Synthesis plans typically use INST/TNM syntax. See TNM for more information.

How to Use Wildcards to Specify Net Names

The wildcard characters, asterisk (*) and question mark (?), enable you to select a group of symbols whose output net names match a specific string or pattern. The asterisk (*) represents any string of zero or more characters. The question mark (?) indicates a single character.

For example, DATA* indicates any net name that begins with “DATA,” such as DATA, DATA1, DATA22, DATABASE, and so on. The string NUMBER? specifies any net names that begin with “NUMBER” and end with one single character, for example, NUMBER1 or NUMBERS, but not NUMBER or NUMBER12.

You can also specify more than one wildcard character. For example, *AT? specifies any net names that begin with any series of characters followed by “AT” and end with any one character such as BAT1, CAT2, and THAT5. If you specify *AT*, you would match BAT11, CAT26, and THAT50.

Pattern Matching Syntax

The syntax for creating a group using pattern matching is:

UCF syntax

```
TIMEGRP “group_name”=predefined_group(“pattern”);
```

where

- *predefined_group* can only be one of the following predefined groups: FFS, LATCHES, PADS, RAMS, CPUS, HSIOS, DSPS, BRAM_PORTA, BRAM_PORTB, or MULTS. (These groups are defined in the section entitled “UCF/NCF,” in the discussion of TNM_NET.)

- *pattern* is any string of characters used in conjunction with one or more wildcard characters.

When specifying a net name, you must use its full hierarchical path name so PAR can find the net in the flattened design.

For FFS, RAMs, LATCHES, PADS, CPUS, DSPS, HSIOS, and MULTS, specify the output net name. For pads, specify the external net name.

Example

The following example illustrates creating a group that includes the flip-flops that source nets whose names begin with $1I3/FRED.

UCF syntax

```
TIMEGRP "group1"=ffs("$1I3/FRED*");
```

Example

The following example illustrates a group that excludes certain flip-flops whose output net names match the specified pattern.

UCF syntax

```
TIMEGRP "this_group"=ffs EXCEPT ffs("a*");
```

In this example, `this_group` includes all flip-flops except those whose output net names begin with the letter "a."

Example

The following example defines a group named "some_latches".

UCF syntax

```
TIMEGRP "some_latches"=latches("$113/xyz*");
```

The group **some_latches** contains all input latches whose output net names start with "$1I3/xyz."

Additional Pattern Matching Details

In addition to using pattern matching when you create timing groups, you can specify a predefined group qualified by a pattern any place you specify a predefined group. The syntax below illustrates how pattern matching can be used within a timing specification.

UCF syntax

```
TIMESPEC "TSidentifier"=FROM predefined_group("pattern") TO
predefined_group
("pattern") value;
```

Patterns Separated by Colon

Instead of specifying just one pattern, you can also specify a list of patterns separated by a colon as illustrated below:

UCF syntax

```
TIMEGRP "some_ffs"=ffs("a*:b?:c*d");
```

The group `some_ffs` contains flip-flops whose output net names adhere to one of the following rules.

- Start with the letter “a”
- Contain two characters; the first character is “b”
- Start with “c” and end with “d”

Defining Area Groups Using Timing Groups

For a complete description, see “AREA_GROUP -- Defining From Timing Groups”.

TIMEGRP Propagation Rules

Applies to all elements or nets within the group.

TIMEGRP Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF

```
TIMEGRP “newgroup”=”existing_grp1” “existing_grp2” [“existing_grp3” .
. .];
```

where *newgroup* is a newly created group that consists of existing groups created via TNMs, predefined groups, or other TIMEGRP attributes.

UCF syntax:

```
TIMEGRP “GROUP1” = “gr2” “GROUP3”;
TIMEGRP “GROUP3” = FFS except “grp5”;
```

NCF

Not applicable.

XCF

XST supports TIMEGRP with the following limitations:

- Groups Creation by Exclusion is not supported
- When a group is defined on the basis of another user group with pattern matching;

  TIMEGRP TG1 = FFS (machine*); # Supported

  TIMEGRP TG2 = TG1 (machine_clk1*); # Not supported

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

In the Advanced tab, click Create next to “Group elements by element output net name” and fill out the Time Group dialog box.

PCF

TIMEGRP *name*;

TIMEGRP *name* = *list of elements*;

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

TIMESPEC

TIMESPEC Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

TIMESPEC Applicable Elements

TS identifiers

TIMESPEC Description

TIMESPEC is a basic timing related constraint. TIMESPEC serves as a placeholder for timing specifications, which are called TS attribute definitions. Every TS attribute begins with the letters “TS” and ends with a unique identifier that can consist of letters, numbers, or the underscore character (_).

TIMESPEC Propagation Rules

Not applicable.

TIMESPEC Syntax

UCF Syntax

A TS attribute defines the allowable delay for paths in your design. The basic syntax for a TS attribute is:

```
TIMESPEC "TSidentifier"=PERIOD "timegroup_name" value [units];
```

where

- **TS***identifier* is a unique name for the TS attribute
- *value* is a numerical value
- *units* can be ms, us, ps, ns

```
TIMESPEC "TSidentifier"=PERIOD "timegroup_name" "TSidentifier" [* or /]
factor PHASE [+ |-] phase_value [units];
```

Syntax Rules

The following rules apply:

- The *value* parameter defines the maximum delay for the attribute. Nanoseconds are the default units for specifying delay time in TS attributes. You can also specify delay using other units, such as picoseconds or megahertz.
- Keywords, such as FROM, TO, and TS appear in the documentation in upper case. However, you can enter them in the TIMESPEC primitive in either upper or lower case. The characters in the keywords must be all upper case or all lower case. Examples of acceptable keywords are:
  - FROM
  - PERIOD
  - TO
  - from
  - to

  Examples of unacceptable keywords are:
  - From
  - To
  - fRoM
  - tO
- If a TSidentifier name is referenced in a property value, it must be entered in upper case letters. For example, the TSID1 in the second constraint below must be entered in upper case letters to match the TSID1 name in the first constraint.

  ```
  TIMESPEC “TSID1” = FROM “gr1” TO “gr2” 50;
  TIMESPEC “TSMAIN” = FROM “here” TO “there” TSID1 /2
  ```
- A colon may be used as a separator instead of a space in all timing specifications.

TIMESPEC FROM-TO Syntax

Within TIMESPEC, you use the following UCF syntax to specify timing requirements between specific end points.

```
TIMESPEC "TSidentifier"=FROM "source_group" TO "dest_group" value
units;
TIMESPEC "TSidentifier"=FROM "source_group" value units;
TIMESPEC "TSidentifier"=TO "dest_group" value units;
```

Unspecified FROM or TO, as in the second and third syntax statements, implies all points.

Note: Although you can use a FROM or TO statement to imply all points, you cannot use an unspecified THRU statement by itself to imply all points.

The From-To statements are TS attributes that reside in the TIMESPEC primitive. The parameters *source_group* and *dest_group* must be one of the following:

- Predefined groups
- Previously created TNM identifiers
- Groups defined in TIMEGRP symbols
- TPSYNC groups

Predefined groups consist of FFS, LATCHES, RAMS, PADS, CPUS, DSPS, HSIOS, BRAMS_PORTA, BRAMS_PORTB, and MULTS. These groups are defined in the section entitled "UCF / NCF," in the discussion of TNM_NET, and are discussed in "Grouping Constraints" of the Constraints Type chapter.

Keywords, such as FROM, TO, and TS appear in the documentation in upper case. However, you use them TIMESPEC in either upper or lower case. You cannot enter them in a combination of lower and upper case.

The *value* parameter defines the maximum delay for the attribute. Nanoseconds are the default units for specifying delay time in TS attributes. You can also specify delay using other units, such as picoseconds or megahertz.

TIMESPEC Examples of FROM-TO TS Attributes

The following examples illustrate the use of From-To TS attributes.

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

```
TIMESPEC "TS_master"=PERIOD "master_clk" 50 HIGH 30;
TIMESPEC "TS_THIS"=FROM FFS TO RAMS 35;
TIMESPEC "TS_THAT"=FROM PADS TO LATCHES 35;
```

XCF

Not applicable.

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints. In the online help index for the Constraints Editor, double-click “TIMESPEC”.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

TNM

TNM Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

TNM Applicable Elements

You can attach TNM constraints to a net, an element pin, a primitive, or a macro.

You can attach the TNM constraint to the net connected to the pad component in a UCF file. NGDBuild transfers the constraint from the net to the pad instance in the NGD file so that it can be processed by the mapper. Use the following UCF syntax:

```
NET "net_name" TNM="property_value";
```

TNM Description

TNM is a basic grouping constraint. Use TNM (Timing Name) to identify the elements that make up a group which you can then use in a timing specification.

TNM tags specific FFS, RAMs, LATCHES, PADS, CPUS, HSIOS, and MULTS as members of a group to simplify the application of timing specifications to the group.

The RISING and FALLING keywords may also be used with TNMs.

TNM Propagation Rules

When attached to a net or signal, TNM propagates to all synchronous elements driven by that net. No special propagation is required.

When attached to a design element, TNM propagates to all applicable elements in the hierarchy within the design element.

The following rules apply to TNMs.

- TNMs applied to pad nets *will not* propagate forward through IBUFs. The TNM is applied to the external pad. This case includes the net attached to the D input of an IFD. See "TNM_NET" if you want the TNM to trace forward from an input pad net.
- TNMs applied to an IBUF instance are illegal.
- TNMs applied to the output pin of an IBUF will propagate the TNM to the next appropriate element.
- TNMs applied to an IBUF element stay attached to that element.
- TNMs applied to a clock-pad-net will not propagate forward through the clock buffer.
- When TNM is applied to a macro, all the elements in the macro will have that timing name.

Special rules apply when using TNM with the PERIOD constraint for Virtex, Virtex-II, Spartan-II CLKDLLs and CLKDLLHFs, and related architectures.

Placing TNMs on Nets

You can place TNM on any net in the design. The constraint indicates that the TNM value should be attached to all valid elements fed by all paths that fan forward from the tagged net. Forward tracing stops at FFS, RAMS, LATCHES, PADS, CPUS, HSIOS, and MULTS. TNMs do not propagate across IBUFs if they are attached to the input pad net.

Placing TNMs on Macro or Primitive Pins

You can place TNM on any macro or component pin in the design if the design entry package allows placement of constraints on macro or primitive pins. The constraint indicates that the TNM value should be attached to all valid elements fed by all paths that fan forward from the tagged pin. Forward tracing stops at FFS, RAMS, LATCHES, PADS, CPUS, HSIOS, and MULTS. The following illustration shows the valid elements for a TNM attached to the schematic of a macro pin.

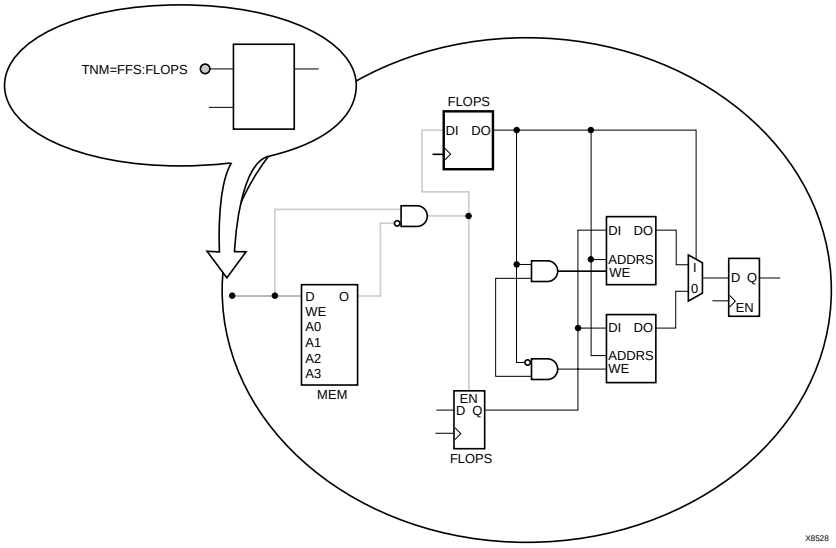


Figure 140-1: **TNM Placed on a Macro Pin**

The syntax for the UCF file is:

```
PIN "pin_name" TNM="FLOPS";
```

Placing TNMs on Primitive Symbols

You can group individual logic primitives explicitly by flagging each symbol, as illustrated by the following figure.

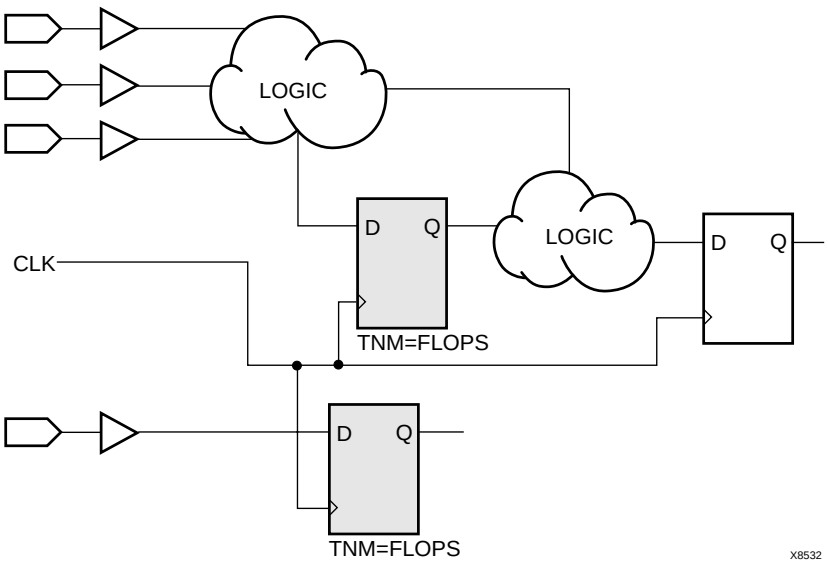


Figure 140-2: **TNM on Primitive Symbols**

In the figure, the flip-flops tagged with the TNM form a group called "'FLOPS." The untagged flip-flop on the right side of the drawing is not part of the group.

Place only one TNM on each symbol, driver pin, or macro driver pin.

Schematic syntax:

```
TNM=FLOPS;
```

UCF syntax

```
INST "instance_name" TNM=FLOPS;
```

Placing TNMs on Macro Symbols

A macro is an element that performs some general purpose higher level function. It typically has a lower level design that consists of primitives, other macros, or both, connected together to implement the higher level function. An example of a macro function is a 16-bit counter.

A TNM constraint attached to a macro indicates that all elements inside the macro (at all levels of hierarchy below the tagged macro) are part of the named group.

When a macro contains more than one symbol type and you want to group only a single type, use the TNM identifier in conjunction with one of the predefined groups: FFS, RAMS, LATCHES, PADS, CPUS, HSIOS, DSPS, BRAM_PORTA, BRAM_PORTB, and MULTS as indicated by the following syntax examples.

UCF syntax:

```
INST "instance_name" TNM=FFS identifier;
INST "instance_name" TNM=RAMS identifier;
INST "instance_name" TNM=LATCHES identifier;
INST "instance_name" TNM=PADS identifier;
INST "instance_name" TNM=CPUS identifier;
INST "instance_name" TNM=HSIOS identifier;
INST "instance_name" TNM=MULTS identifier;
```

If multiple symbols of the same type are contained in the same hierarchical block, you can simply flag that hierarchical symbol, as illustrated by the following figure. In the figure, all flip-flops included in the macro are tagged with the TNM "FLOPS". By tagging the macro symbol, you do not have to tag each underlying symbol individually.

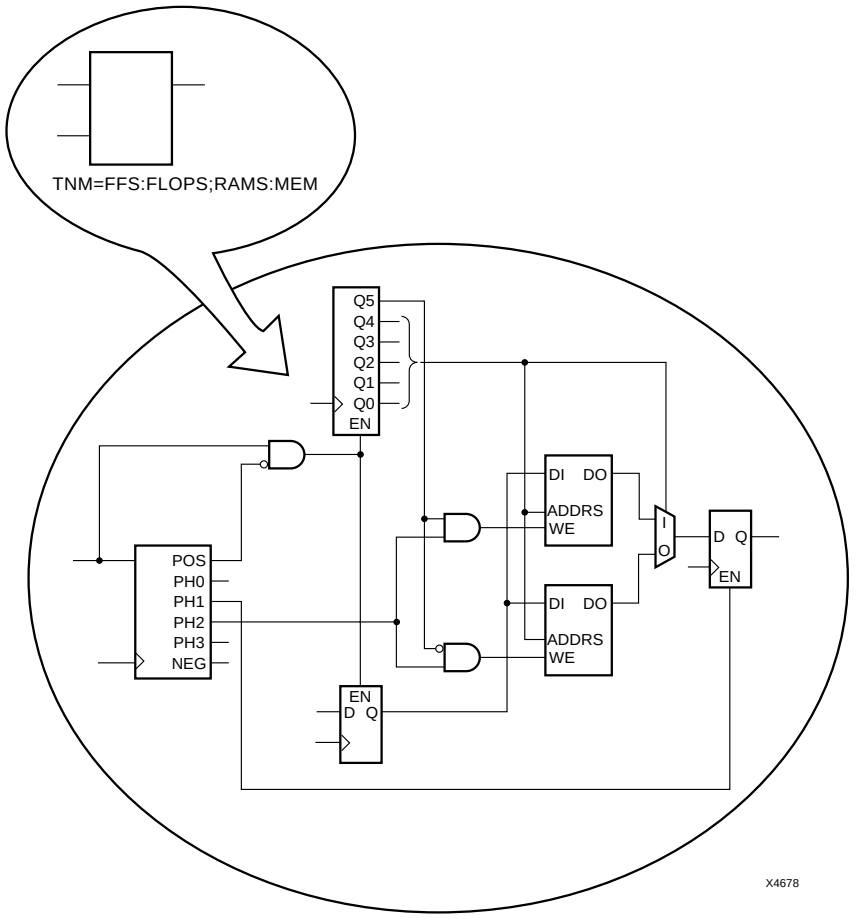


Figure 140-3: **TNM on Macro Symbol**

Placing TNMs on Nets or Pins to Group Flip-Flops and Latches

You can easily group flip-flops, latches, or both by flagging a common input net, typically either a clock net or an enable net. If you attach a TNM to a net or driver pin, that TNM applies to all flip-flops and input latches that are reached through the net or pin. That is, that path is traced forward, through any number of gates or buffers, until it reaches a flip-flop or input latch. That element is added to the specified TNM group.

The following figure illustrates the use of a TNM on a net that traces forward to create a group of flip-flops.

In the figure, the constraint TNM=FLOPS traces forward to the first two flip-flops, which form a group called FLOPS. The bottom flip-flop is not part of the group FLOPS.

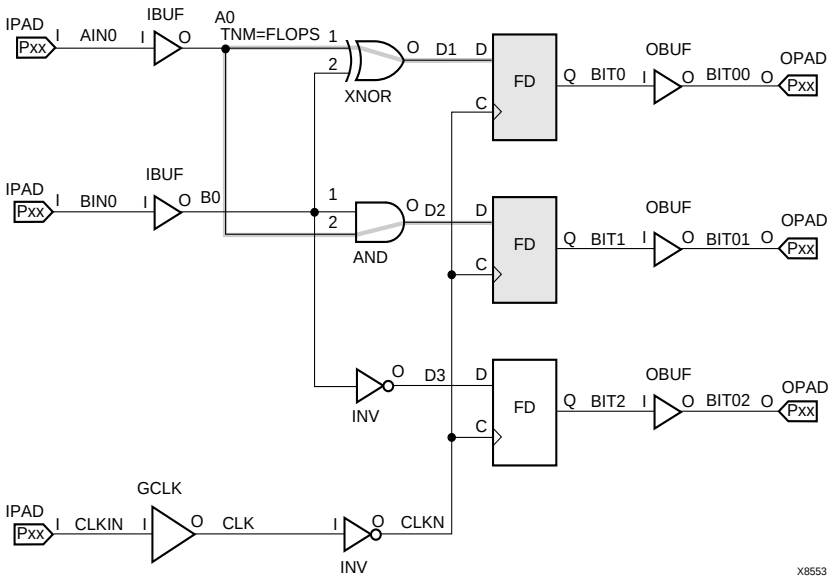


Figure 140-4: **TNM on Net Used to Group Flip-Flops**

The following figure illustrates placing a TNM on a clock net, which traces forward to all three flip-flops and forms the group Q_FLOPS.

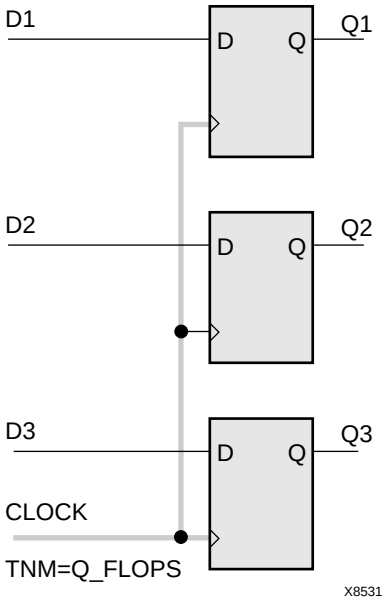


Figure 140-5: **TNM on Clock Pin Used to Group Flip-Flops**

The TNM parameter on nets or pins is allowed to have a qualifier.

For example, on schematics:

```
TNM=FFS data;
TNM=RAMS fifo;
TNM=LATCHES capture;
```

In UCF files

```
{NET | PIN} "net_or_pin_name" TNM=FFS data;
{NET | PIN} "net_or_pin_name" TNM=RAMS fifo;
{NET | PIN} "net_or_pin_name" TNM=LATCHES capture;
```

A qualified TNM is traced forward until it reaches the first storage element (FFS, RAMS, LATCHES, PADS, CPUS, HSIOS, and MULTS). If that type of storage element matches the qualifier, the storage element is given that TNM value. Whether or not there is a match, the TNM is *not* traced through that storage element.

TNM parameters on nets or pins are never traced through a storage element (FFS, RAMS, LATCHES, PADS, CPUS, HSIOS, and MULTS).

TNM Syntax Examples

Schematic

Attach to a net or a macro.

Attribute Name—TNM

Attribute Values—*identifier*

See the UCF section for a discussion of *identifier*.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

```
XILINX PROPERTY 'TNM=identifier mysignal';
```

UCF/NCF

```
{NET | PIN} "net_or_pin_name" TNM=[predefined_group:] identifier;
```

where

predefined_group can be

- all of the members of a predefined group using the keywords FFS, RAMS, LATCHES, PADS, CPUS, HSIOS, and MULTS as follows:
  - FFS refers to all CLB and IOB flip-flops. (Flip-flops built from function generators are not included.)
  - RAMS refers to all RAMs for architectures with RAMS. This includes LUT RAMS and BLOCK RAMS.
  - PADS refers to all I/O pads.

- LATCHES refers to all CLB or IOB latches. (Latches built from function generators are not included.)
- MULTS group the Spartan-3 and Virtex-II registered multiplier.
- CPUS group the Virtex-II Pro or Virtex-II Pro X processor.
- HSIOS to group the Virtex-II Pro or Virtex-II Pro X gigabit transceiver.

- a subset of elements in a group predefined by name matching using the following syntax:

  predefined_group (name_qualifier1... name_qualifiern)

where

identifier can be any combination of letters, numbers, or underscores.

Do not use the reserved words FFS, RAMS, LATCHES, PADS, CPUS, HSIOS, MULTS, RISING, FALLING, TRANSHI, TRANSLO, or EXCEPT as *identifiers.*

The constraints in the table below are also reserved words and should not be used as *identifiers*.

Reserved Words (Constraints)		
ADD	FAST	NODELAY
ALU	FBKINV	OPT
ASSIGN	FILE	OSC
BEL	F_SET	RES
BLKNM	HBLKNM	RLOC
CAP	HU_SET	RLOC_ORIGIN
CLKDV_DIVIDE	H_SET	RLOC_RANGE
CLBNM	INIT	SCHNM
CMOS	INIT OX	SLOW
CYMODE	INTERNAL	STARTUP_WAIT
DECODE	IOB	SYSTEM
DEF	IOSTANDARD	TNM
DIVIDE1_BY	LIBVER	TRIM
DIVIDE2_BY	LOC	TS
DOUBLE	LOWPWR	TTL
DRIVE	MAP	TYPE
DUTY_CYCLE_ CORRECTION	MEDFAST	USE_RLOC
	MEDSLOW	U_SET
	MINIM	

You can specify as many groups of end points as are necessary to describe the performance requirements of your design. However, to simplify the specification process and reduce the place and route time, use as few groups as possible.

XCF

See the UCF section.

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

In the Advanced tab, click Create next to “Group elements by instance name” or Create next to “Group elements by hierarchy” and fill out the Time Name dialog box.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

TNM_NET

TNM_NET Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

TNM_NET Applicable Elements

Nets

TNM_NET Description

TNM_NET is a basic grouping constraint. TNM_NET (timing name for nets) identifies the elements that make up a group, which can then be used in a timing specification. TNM_NET is essentially equivalent to TNM on a net *except* for input pad nets. (Special rules apply when using TNM_NET with the PERIOD constraint for DLL/DCMs. See "PERIOD Specifications on CLKDLLs and DCMs".)

A TNM_NET is a property that you normally use in conjunction with an HDL design to tag a specific net. All downstream synchronous elements and pads tagged with the TNM_NET identifier are considered a group.

TNM_NET (Timing Name - Net) tags specific synchronous elements, pads, and latches as members of a group to simplify the application of timing specifications to the group. NGDBuild never transfers a TNM_NET constraint from the attached net to an input pad, as it does with the TNM constraint.

TNM_NET Rules

The following rules apply to TNM_NET:

- TNM_NETs applied to pad nets propagate forward through the IBUF or OBUF and any other combinatorial logic to synchronous logic or pads.
- TNM_NETs applied to a clock-pad-net propagate forward through the clock buffer.
- Special rules apply when using TNM_NET with the PERIOD constraint for Virtex, Spartan-II, Virtex-II Pro, Virtex-II Pro X, and Virtex-4 DLL and DCMs.

Use TNM_NET to define certain types of nets that cannot be adequately described by the TNM constraint.

For example, consider the following design.

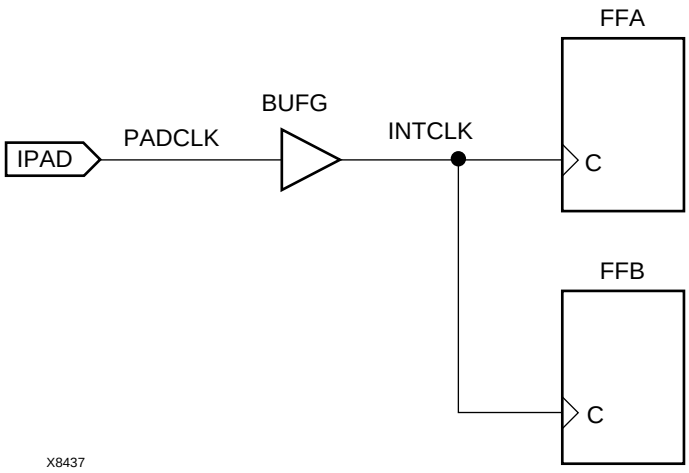


Figure 141-1: **TNM Associated with the IPAD**

In the preceding design, a TNM associated with the IPAD symbol only includes the PAD symbol as a member in a timing analysis group. For example, the following UCF file entry creates a time group that includes the IPAD symbol only.

```
NET “PADCLK” TNM= “PADGRP”; (UCF file example)
```

However, using TNM to define a time group for the net PADCLK creates an empty time group.

```
NET “PADCLK” TNM=FFS(*) “FFGRP”;(UCF file example)
```

All properties that apply to a pad are transferred from the net to the PAD symbol. Since the TNM is transferred from the net to the PAD symbol, the qualifier, “FFS(*)” does not match the PAD symbol.

To overcome this obstacle for schematic designs using TNM, you can create a time group for the INTCLK net.

```
NET “INTCLK” TNM=FFS(*) FFGRP;(UCF file example)
```

However, for HDL designs, the only meaningful net names are the ones connected directly to pads. Then, use TNM_NET to create the FFGRP time group.

```
NET PADCLK TNM_NET=FFS(*) FFGRP;(UCF file example)
```

NGDBuild does not transfer a TNM_NET constraint from a net to an IPAD as it does with TNM.

You can use TNM_NET in NCF or UCF files as a property attached to a net in an input netlist (EDIF or NGC). TNM_NET is not supported in PCF files.

You can only use TNM_NET with nets. If TNM_NET is used with any other object such as a pin or symbol, a warning is generated and the TNM_NET definition is ignored.

TNM_NET Propagation Rules

It is illegal to attach TNM_NET to a design element.

TNM_NET Syntax Examples

Schematic

Attach to a net.

Attribute Name—TNM_NET

Attribute Values—*identifier*

See the UCF section for a discussion of *identifier.*

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

```
NET “net_name” TNM_NET=[predefined_group:]identifier;
```

where

predefined_group can be

- all of the members of a predefined group using the keywords FFS, RAMS, PADS, MULTS, HSIOS, CPUS, DSPS, BRAMS_PORTA, BRAMS_PORTB or LATCHES as follows:
  - FFS refers to all CLB and IOB flip-flops. (Flip-flops built from function generators are not included.)
  - RAMS refers to all RAMs for architectures with RAMS. This includes LUT RAMS and BLOCK RAMS.

- PADS refers to all I/O pads.
- MULTS group the Spartan-3 and Virtex-II registered multiplier.
- CPUS group the Virtex-II Pro or Virtex-II Pro X processor.
- DSPS is used to group DSP elements like the Virtex-4 DSP48.
- HSIOS group the Virtex-II Pro or Virtex-II Pro X gigabit transceiver.
- LATCHES refers to all CLB or IOB latches. (Latches built from function generators are not included.)

- a subset of elements in a group predefined by a name using the following syntax:

  predefined_group (name_qualifier1... name_qualifiern)

where

identifier can be any combination of letters, numbers, or underscores. Do not use reserved words, such as FFS, RAMS, PADS, MULTS, HSIOS, CPUS, or LATCHES for TNM_NET identifiers.

The following statement identifies all flip-flops fanning out from the PADCLK net as a member of the timing group GRP1.

```
NET “PADCLK” TNM_NET=FFS(*) ”GRP1”;
```

XCF

XST supports TNM_NET with the following limitation: only a single pattern supported for predefined groups:

The following command syntax is supported:

```
NET “PADCLK” TNM_NET=FFS(*) ”GRP1”;
```

The following command syntax is *not* supported:

```
NET “PADCLK” TNM_NET = FFS(machine/*:xcounter/*) TG1;
```

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

In the Advanced tab, click Create next to “Group elements associated by Nets” and fill out the Time Name dialog box.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

TPSYNC

TPSYNC Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

TPSYNC Applicable Elements

Nets, instances, pins

TPSYNC Description

TPSYNC is an advanced grouping constraint and a modular design constraint. It flags a particular point or a set of points with an identifier for reference in subsequent timing specifications. You can use the same identifier on several points, in which case timing analysis treats the points as a group.

When the timing of a design must be designed from or to a point that is not a synchronous element or I/O pad, the following rules apply if a TPSYNC timing point is attached to a net, macro pin, output or input pin of a primitive, or an instance.

- A net — the source of the net is identified as a potential source or destination for timing specifications.
- A macro pin — all of the sources inside the macro that drive the pin to which the constraint is attached are identified as potential sources or destinations for timing specifications. If the macro pin is an input pin (that is, if there are no sources for the pin in the macro), then all of the load pins in the macro are flagged as synchronous points.

  In the following diagram, POINTY applies to the inverter.

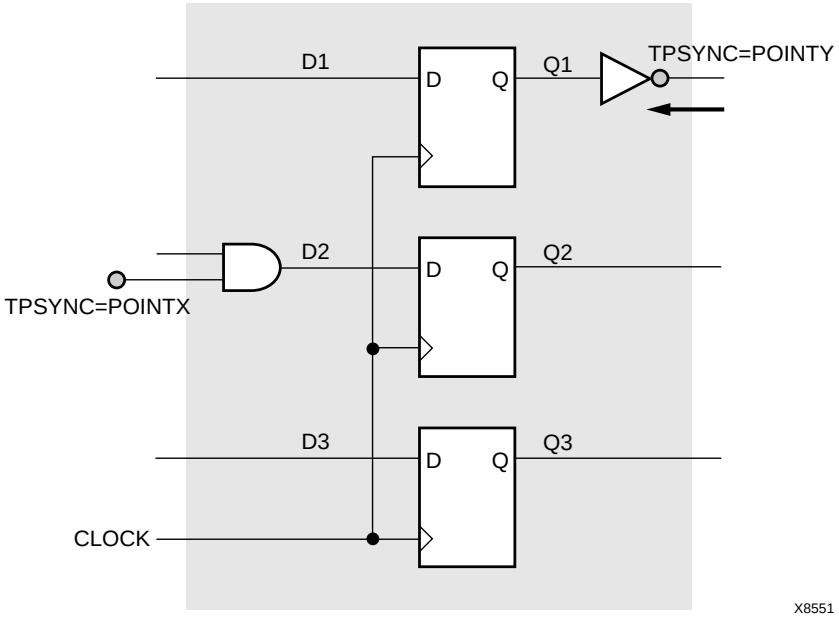


Figure 142-1: **TPSYNCs Attached to Macro Pins**

- The output pin of a primitive — the primitive's output is flagged as a potential source or destination for timing specifications.
- The input pin of a primitive — the primitive's input is flagged as a potential source or destination for timing specifications.
- An instance — the output of that element is identified as a potential source or destination for timing specifications.

- A primitive symbol—Attached to a primitive symbol, TPSYNC identifies the output(s) of that element as a potential source or destination for timing specifications. See the following figure.

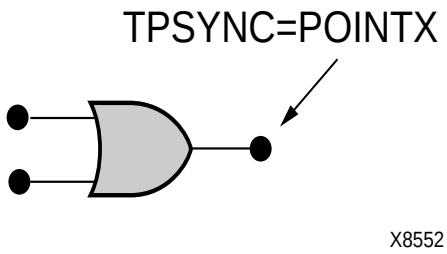


Figure 142-2: **TPSYNC Attached to a Primitive Symbol**

The use of a TPSYNC timing point to define a synchronous point in a design implies that the flagged point cannot be merged into a function generator. For example, consider the following diagram.

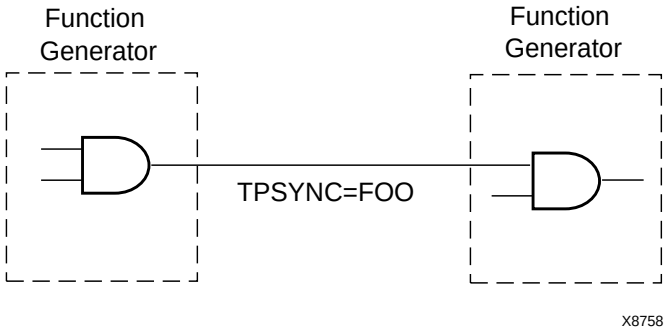


Figure 142-3: **Working with Two Gates**

In this example, because of the TPSYNC definition, the two gates cannot be merged into a single function generator.

TPSYNC Propagation Rules

See "TPSYNC Description" for details.

TPSYNC Syntax Examples

Schematic

Attached to a net, instance, or pin.

Attribute Name—TPSYNC

Attribute Values—*identifier*

where *identifier* is a name that is used in timing specifications in the same way that groups are used.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

```
NET “net_name” TPSYNC=identifier;
INST “instance_name” TPSYNC=identifier;
PIN “pin_name” TPSYNC=identifier;
```

where *identifier* is a name that is used in timing specifications in the same way that groups are used.

All flagged points are used as a source or destination or both for the specification where the TPSYNC identifier is used.

The name for the identifier must be unique to any identifier used for a TNM or TNM_NET grouping constraint.

The following statement identifies latch as a potential source or destination for timing specifications for the net logic_latch.

```
NET “logic_latch” TPSYNC=latch;
```

XCF

Not yet supported.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

TPSYNC for Modular Designs

The NET/TPSYNC UCF constraint has the following syntax:

```
NET "net_name" TPSYNC="group_name";
```

This constraint specifies that either all drivers or loads on the net *net_name* should be saved and added to the timegroup *group_name*. The synchronization names on these drivers or loads can then be referenced in other timing specifications such as OFFSET or FROM/TO constraints. This constraint will be translated into a TIMEGRP/PIN constraint in the PCF file. This constraint has the following syntax:

```
TIMEGRP "group_name"=PIN "pseudo_comp";
```

The *pseudo_comp* argument is the component created by the mapper to represent the dangling endpoint of the port net *net_name*. Within the modular design flow the NET/TPSYNC constraint is used with the OFFSET/OUT or OFFSET/IN constraint to specify the timing to or from a module port.

For nets, the behavior is true *only* if the named net is

a. Connected to the port of an active module (in active module implementation mode), and

b. Is *not* connected to any logic in the context design.

Only if these requirements are met will the port's pseudo logic be put into the named group. If (a) is not met, the net's driver will be put into the TPSYNC group, which is the usual behavior of TPSYNC. If (b) is not met, the mapper will discard the TPSYNC on that net, with a warning.

TPSYNC can also be used for the "pad group" in the OFFSET constraint. Following are some examples of TPSYNC use:

```
NET "module_input1" TPSYNC="MODULE_IN"; // two module ports
NET "module_input2" TPSYNC="MODULE_IN"; // in one group
NET "module_output" TPSYNC="MODULE_OUT";
TIMEGRP "MODULE_IN" OFFSET=IN 5 nS BEFORE "CLK"; // setup to module input
TIMEGRP "MODULE_OUT" OFFSET=OUT 5 nS AFTER "CLK"; // clock to module output
TIMESPEC TS1=FROM MODULE_IN TO MODULE_OUT 7 nS; // or combinatorial path
```

TPTHRU

TPTHRU Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

TPTHRU Applicable Elements

- Nets
- Pins
- Instances

TPTHRU Description

TPTHRU is an advanced grouping constraint. It flags a particular point or a set of points with an identifier for reference in subsequent timing specifications. If you use the same identifier on several points, timing analysis treats the points as a group. See “TIMESPEC”.

Use the TPTHRU constraint when it is necessary to define intermediate points on a path to which a specification applies. See “TSidentifier”.

TPTHRU Propagation Rules

Not applicable.

TPTHRU Syntax Examples

Schematic

Attach to a net, instance, or pin.

Attribute Name—TPTHRU

Attribute Values—*identifier*

See the UCF section for a discussion of *identifier*.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is as follows:

```
NET “net_name” TPTHRU=identifier;
INST “instance_name” TPTHRU=identifier;
PIN “instance_name.pin_name” TPTHRU=”thru_group_name”;
```

where

identifier is a name used in timing specifications for further qualifying timing paths within a design.

The name for the identifier must be different from any identifier used for a TNM constraint.

Using TPTHRU in a FROM TO Constraint

It is sometimes convenient to define intermediate points on a path to which a specification applies. This defines the maximum allowable delay and has the syntax shown in the following sections.

UCF Syntax with TIMESPEC

```
TIMESPEC “TSidentifier”=FROM “source_group” THRU “thru_point” [THRU
“thru_point”] TO “dest_group” allowable_delay [units];
TIMESPEC “TSidentifier”=FROM “source_group” THRU “thru_point” [THRU
“thru_point”] allowable_delay [units];
```

where

- *identifier* is an ASCII string made up of the characters A..Z, a..z, 0..9, and underscore (_).
- *source_group* and *dest_group* are user-defined groups, predefined groups or TPSYNCs.
- *thru_point* is an intermediate point used to qualify the path, defined using a TPTHRU constraint.
- *allowable_delay* is the timing requirement.
- *units* is an optional field to indicate the units for the allowable delay. Default units are nanoseconds, but the timing number can be followed by ps, ns, us, ms, GHz, MHz, or KHz to indicate the intended units.

The example shows how to use the TPTHRU constraint with the THRU constraint on a schematic. The UCF syntax is as follows.

```
INST “FLOPA” TNM=”A”;
INST “FLOPB” TNM=”B”;

NET “MYNET” TPTHRU=”ABC”;
TIMESPEC “TSpath1”=FROM “A” THRU “ABC” TO “B” 30;
```

The following schematic shows the placement of the TPTHRU constraint and the resultant path that is defined.

The following statement identifies the net on_the_way as an intermediate point on a path to which the timing specification named “here” applies.

```
NET “on_the_way” TPTHRU=”here”;
```

Note: The following NCF construct is not supported.

```
TIMESPECT “TS_1”=THRU “Thru_grp” 30.0
```

XCF

Not yet supported.

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

In the Advanced tab, click Create next to “Timing THRU Points (TPTHRU)” and then fill out the Timing THRU Point dialog box.

PCF

```
PATH "name"=FROM "source" THRU "thru_pt1" ...THRU "thru_ptn" TO
"destination";
```

You are not required to have a FROM, THRU, and TO. You can basically have any combination (FROM-TO, FROM-THRU-TO, THRU-TO, TO, FROM, FROM-THRU-THRU-THRU-TO, FROM-THRU, and so on). There is no restriction on the number of THRU points. The source, thru points, and destination can be a net, bel, comp, macro, pin, or timegroup.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

TRANSLATE_OFF and TRANSLATE_ON

TRANSLATE_OFF and TRANSLATE_ON Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

TRANSLATE_OFF and TRANSLATE_ON Applicable Elements

TRANSLATE_OFF and TRANSLATE_ON can be applied locally only.

TRANSLATE_OFF and TRANSLATE_ON Description

TRANSLATE_OFF and TRANSLATE_ON are synthesis constraints. Use TRANSLATE_OFF and TRANSLATE_ON to instruct XST to ignore portions of your VHDL or Verilog code that are not relevant for synthesis—for example, simulation code. The TRANSLATE_OFF directive marks the beginning of the section to be ignored and the translate_on directive instructs XST to resume synthesis from that point.

Note: The constraints TRANSLATE_OFF and TRANSLATE_ON are also Synplicity and Synopsys constraints that are supported by XST in Verilog. Automatic conversion is also available in VHDL and Verilog.

Note: translate_on/translate_off could be used with the following words:

- synthesis

- synopsys
- pragma

TRANSLATE_OFF and TRANSLATE_ON Propagation Rules

Instructs synthesis tool to enable or disable portions of code.

TRANSLATE_OFF and TRANSLATE_ON Syntax Examples

Schematic

Not applicable.

VHDL

In your VHDL code, the directives should be written as follows:

```
-- synthesis translate_off
 ...code not synthesized...
-- synthesis translate_on
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

The directives are available as VHDL or Verilog meta comments. The Verilog syntax differs from the standard meta comment syntax presented earlier in this chapter, as shown below.

```
// synthesis translate_off
...code not synthesized...
// synthesis translate_on
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

TRISTATE2LOGIC

TRISTATE2LOGIC Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	No
Spartan-3E	No
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	No
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner II	No

TRISTATE2LOGIC Applicable Elements

This constraint can be applied to an entire design via an XST command line, to a particular block (entity, architecture, component), and to a signal.

TRISTATE2LOGIC Description

TRISTATE2LOGIC is a synthesis constraint that allows you to transform internal tristates to logic. Replacing internal tristates by logic allows you to make additional logic optimization that brings additional speed design improvements. In general tristate to logic replacement may lead to area increase. You should set tristate2logic=no if the optimization goal is Area.

Limitations:

- Only internal tristates are replaced by logic, which means that the tristates of the top module connected to output pads are preserved.

- Internal tristates are not replaced by logic for modules when incremental synthesis is active.
- This switch does not apply to technologies that do not have internal tristates, like Spartan-3 or Virtex-4 devices. In this case, the conversion of tristates to logic is performed automatically. Please note, that in some situations XST is not able to make the replacement automatically, due to the fact that this may lead to wrong design behavior or multi-source. This may happen when the hierarchy is preserved or XST does not have full design visibility (for example, design is synthesized on a block-by-block basis). In these cases XST gives a warning message at low level optimization step. Depending on the particular design situation, you may continue the design flow and the replacement could be done by MAP, or you can force the replacement by applying tristate2logic = yes constraint on a particular block or signal. Please refer to Answer Record #20048 for more information.

Allowed values are YES and NO (TRUE and FALSE are available in XCF as well). By default, tristate to logic transformation is enabled (YES).

TRISTATE2LOGIC Propagation Rules

Applies to an entity, component, module, or signal to which it is attached.

TRISTATE2LOGIC Syntax Examples

Schematic

Not applicable.

VHDL

Before using TRISTATE2LOGIC, declare it with the following syntax:

```
attribute tristate2logic: string;
```

After TRISTATE2LOGIC has been declared, specify the VHDL constraint as follows:

```
attribute tristate2logic of {entity_name|component_name|signal_name}:
{entity|component|signal} is "yes";
```

For a more detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute tristate2logic [of] {module_name|signal_name}
[is] “yes”;
```

For a more detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL "entity_name" tristate2logic={yes|no|true|false};
BEGIN MODEL "entity_name"
  NET "signal_name" tristate2logic={yes|no|true|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-tristate2logic** command line option of the **run** command. Following is the basic syntax:

```
-tristate2logic {YES|NO}
```

The default is **YES**.

Project Navigator

Set TRISTATE2LOGIC, globally with the Convert Tristates To Logic option in the Xilinx Specific Options tab of the Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

TSidentifier

TSidentifier Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	Yes
CoolRunner XPLA3	Yes
CoolRunner-II	Yes

TSidentifier Applicable Elements

TIMESPEC keywords

TSidentifier Description

TS*identifier* is a basic timing constraint. TS*identifier* properties beginning with the letters “TS” are used with the TIMESPEC keyword in a UCF file. The value of TS*identifier* corresponds to a specific timing specification that can then be applied to paths in the design.

TSidentifier Propagation Rules

It is illegal to attach TS*identifier* to a net, signal, or design element.

All the following syntax definitions use a space as a separator. The use of a colon (:) as a separator is optional.

TSidentifier Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

Defining a Maximum Allowable Delay

```
TIMESPEC "TSidentifier"=[MAXDELAY] FROM "source_group" TO "dest_group"
allowable_delay [units];
```

or

```
TIMESPEC "TSidentifier"=FROM "source_group" TO "dest_group"
allowable_delay [units];
```

Defining Intermediate Points (UCF)

```
TIMESPEC "TSidentifier"=FROM "source_group" THRU "thru_point" [THRU
"thru_point1"... "thru_pointn"] TO "dest_group" allowable_delay
[units];
```

where

- *identifier* is an ASCII string made up of the characters A-Z, a-z, 0-9, and _
- *source_group* and *dest_group* are user-defined or predefined groups
- *thru_point* is an intermediate point used to qualify the path, defined using a TPTHRU constraint
- *allowable_delay* is the timing requirement value
- *units* is an optional field to indicate the units for the allowable delay. The default units are nanoseconds (ns), but the timing number can be followed by ps, ns, us, ms, GHz, MHz, or kHz to indicate the intended units.

Defining a Linked Specification

This allows you to link the timing number used in one specification to another specification.

```
TIMESPEC "TSidentifier"=FROM "source_group" TO "dest_group"
another_TSid[/ | *] number;
```

where

- *identifier* is an ASCII string made up of the characters A-Z, a-z, 0-9, and _

- *source_group* and *dest_group* are user-defined or predefined groups
- *another_Tsid* is the name of another timespec
- *number* is a floating point number

Defining a Clock Period

This allows more complex derivative relationships to be defined as well as a simple clock period.

```
TIMESPEC "TSidentifier"=PERIOD "TNM_reference" value [units] [{HIGH |
LOW} [high_or_low_time [hi_lo_units]]];INPUT_JITTER
```

where

- *identifier* is a reference identifier with a unique name.
- *TNM_reference* is the identifier name attached to a clock net (or a net in the clock path) using a TNM constraint.
- *value* is the required clock period.
- *units* is an optional field to indicate the units for the allowable delay. The default units are nanoseconds (ns), but the timing number can be followed by us, ms, ps, ns, GHz, MHz, or kHz to indicate the intended units.
- HIGH or LOW can be optionally specified to indicate whether the first pulse is to be High or Low.
- *high_or_low_time* is the optional High or Low time, depending on the preceding keyword. If an actual time is specified, it must be less than the period. If no High or Low time is specified, the default duty cycle is 50 percent.
- *hi_lo_units* is an optional field to indicate the units for the duty cycle. The default is nanoseconds (ns), but the High or Low time number can be followed by ps, us, ms, ns or % if the High or Low time is an actual time measurement.

Specifying Derived Clocks

```
TIMESPEC "TSidentifier"=PERIOD "TNM_reference"
"another_PERIOD_identifier" [/ | *] number [{HIGH | LOW}
[high_or_low_time [hi_lo_units]]];INPUT_JITTER
```

where

- *TNM_reference* is the identifier name attached to a clock net (or a net in the clock path) using a TNM constraint.
- *another_PERIOD_identifier* is the name of the identifier used on another period specification.
- *number* is a floating point number.
- HIGH or LOW can be optionally specified to indicate whether the first pulse is to be High or Low.
- *high_or_low_time* is the optional High or Low time, depending on the preceding keyword. If an actual time is specified, it must be less than the period. If no High or Low time is specified, the default duty cycle is 50 percent.
- *hi_lo_units* is an optional field to indicate the units for the duty cycle. The default is nanoseconds (ns), but the High or Low time number can be followed by ps, us, ms, or % if the High or Low time is an actual time measurement.

Ignoring Paths

Note: This form is not supported for CPLDs.

There are situations in which a path that exercises a certain net should be ignored because all paths through the net, instance, or instance pin are not important from a timing specification point of view.

```
TIMESPEC "TSidentifier"=FROM "source_group" TO "dest_group" TIG;
```

or

```
TIMESPEC "TSidentifier"=FROM "source_group" THRU "thru_point" [THRU
"thru_point1"... "thru_pointn"]TO "dest_group" TIG;
```

where

- *identifier* is an ASCII string made up of the characters A-Z, a-z 0-9, and _
- *source_group* and *dest_group* are user-defined or predefined groups
- *thru_point* is an intermediate point used to qualify the path, defined using a TPTHRU constraint

The following statement says that the timing specification TS_35 calls for a maximum allowable delay of 50 ns between the groups “here” and “there”.

```
TIMESPEC "TS_35"=FROM "here" TO "there" 50;
```

The following statement says that the timing specification TS_70 calls for a 25 ns clock period for clock_a, with the first pulse being High for a duration of 15 ns.

```
TIMESPEC "TS_70"=PERIOD "clock_a" 25 high 15;
```

For more information, see “Logical and Physical Constraints”.

XCF

Not applicable.

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

You can enter clock period timing constraints in the Global tab. Input setup time and clock-to-output delay can be entered for specific pads in the Ports tab, or for all pads related to a given clock in the Global tab. Combinatorial pad-to-pad delays can be entered in the Advanced tab, or for all pad-to-pad paths in the Global tab.

PCF

The same as the UCF syntax without the TIMESPEC keyword.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

To set constraints, in the FPGA Editor main window, click Properties of Selected Items from the Edit menu. With a component, net, path, or pin selected, you can set a TSid from the Physical Constraints tab.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

U_SET

U_SET Architecture Support

Note: The numbers in the table below indicate applicable elements. See "U_SET Applicable Elements" (following).

Architecture	Supported/Unsupported
Virtex	1, 2, 3, 4, 5, 6, 8
Virtex-E	1, 2, 3, 4, 5, 6, 8
Spartan-II	1, 2, 3, 4, 5, 6, 8
Spartan-IIE	1, 2, 3, 4, 5, 6, 8
Spartan-3	1, 2, 3, 4, 5, 7, 9
Spartan-3E	1, 2, 3, 4, 5, 7, 9
Virtex-II	1, 2, 3, 4, 5, 6, 7, 9
Virtex-II Pro	1, 2, 3, 4, 5, 6, 7, 9
Virtex-II Pro X	1, 2, 3, 4, 5, 6, 7, 9
Virtex-4	1, 2, 3, 4, 5, 10, 11
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

U_SET Applicable Elements

1. Registers
2. FMAP
3. Macro Instance
4. ROM
5. RAMS, RAMD
6. BUFT
7. MULT18X18S
8. RAMB4_Sm_Sn, RAMB4_Sn
9. RAMB16_Sm_Sn, RAMB16_Sn
10. RAMB16
11. DSP48

U_SET Description

U_SET is an advanced mapping constraint. It groups design elements with attached RLOC constraints that are distributed throughout the design hierarchy into a single set. The elements that are members of a U_SET can cross the design hierarchy. You can arbitrarily select objects without regard to the design hierarchy and tag them as members of a U_SET. For more information about U_SET, see "U_SET".

U_SET Propagation Rules

U_SET is a macro constraint and any attachment to a net is illegal.

U_SET Syntax Examples

Schematic

Attach to a valid instance.

Attribute Name—U_SET

Attribute Values—*name*

where *name* is the identifier of the set.

VHDL

Before using U_SET, declare it with the following syntax:

```
attribute u_set: string;
```

After U_SET has been declared, specify the VHDL constraint as follows:

```
attribute u_set of {component_name|label_name}: {component|label} is
"name";
```

where *name* is the identifier of the set.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute u_set [of] {module_name|instance_name} [is]
name;
```

where *name* is the identifier of the set.

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name" U_SET=name;
```

where *name* is the identifier of the set.

This name is absolute. It is not prefixed by a hierarchical qualifier.

The following statement specifies that the design element ELEM_1 be in a set called JET_SET.

```
INST “$1I3245/ELEM_1” U_SET=JET_SET;
```

XCF

```
BEGIN MODEL “entity_name”
 INST "instance_name" U_SET=uset_name;
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

USE_CARRY_CHAIN

USE_CARRY_CHAIN Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

USE_CARRY_CHAIN Applicable Elements

Signals, and can be applied globally as well.

USE_CARRY_CHAIN Description

USE_CARRY_CHAIN is a synthesis constraint. This constraint instructs XST to use the dedicated carry chain functionality for the modules listed in the constraint. It is both a global and a local constraint, and has values of Yes or No, with Yes being the default.

USE_CARRY_CHAIN Propagation Rules

Applies to the signal to which it is attached.

USE_CARRY_CHAIN Syntax Examples

Schematic

Attach to a valid instance.

Attribute Name—USE_CARRY_CHAIN

Attribute Value—YES, NO

VHDL

Before using USE_CARRY_CHAIN, declare it with the following syntax:

```
attribute USE_CARRY_CHAIN: string;
```

After USE_CARRY_CHAIN has been declared, specify the VHDL constraint as follows:

```
attribute USE_CARRY_CHAIN of signal_name: signal is "{yes|no}";
```

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
// synthesis attribute USE_CARRY_CHAIN [of] signal_name [is] {yes|no};
```

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

MODEL "entity_name" use_carry_chain={yes | no | true | false};

BEGIN MODEL "entity_name"

NET "signal_name" use_carry_chain={yes | no | true | false};

END;

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the -use_carry_chain command line option of the run command. Following is the basic syntax:

```
-use_carry_chain {YES|NO}
```

The default is YES.

Project Navigator

Not applicable.

USE_CLOCK_ENABLE

USE_CLOCK_ENABLE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner II	No

USE_CLOCK_ENABLE Applicable Elements

This constraint can be applied to an entire design via an XST command line, to a particular block (entity, architecture, component), to a signal representing FF, and to an instance representing instantiated FF.

USE_CLOCK_ENABLE Description

USE_CLOCK_ENABLE is a synthesis constraint that allows you (or prevents) a usage of a clock enable in the design. By detecting this constraint with a value of "no" or "false", XST avoids using CE resources in the final implementation. Moreover, for some designs, putting Clock Enable function on data input of the FF allows better logic optimization and therefore better QOR. In Auto mode XST tries to estimate a trade off between using dedicated CE input of an FF input and putting CE logic on D input of an FF. In a case where an FF is instantiated by the user, XST removes the Clock Enable only if the "Optimize Instantiated Primitives" switch is set to "yes".

Allowed values are AUTO, YES, and NO (TRUE and FALSE ones are available in XCF as well). By default, the usage of clock enable signal is enabled (AUTO).

USE_CLOCK_ENABLE Propagation Rules

Applies to an entity, component, module, signal, or instance to which it is attached.

USE_CLOCK_ENABLE Syntax Examples

Schematic

Not applicable.

VHDL

Before using USE_CLOCK_ENABLE, declare it with the following syntax:

```
attribute use_clock_enable: string;
```

After USE_CLOCK_ENABLE has been declared, specify the VHDL constraint as follows:

```
attribute use_clock_enable of
{entity_name|component_name|signal_name|instance_name}:
{entity|component|signal|label} is "no";
```

For a more detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute use_clock_enable [of]
{module_name|signal_name|isntance_name} [is] no;
```

For a more detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL “entity_name” use_clock_enable={auto|yes|true|no|false};
BEGIN MODEL “entity_name”
  NET “signal_name” use_clock_enable={auto|yes|true|no|false};
  INST “instance_name” use_clock_enable={auto|yes|true|no|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-use_clock_enable** command line option of the **run** command. Following is the basic syntax:

```
-use_clock_enable {AUTO|YES|NO}
```

The default is **AUTO**.

Project Navigator

Set USE_CLOCK_ENABLE globally with the Use Clock Enable option in the Xilinx Specific Options tab of the Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

USE_DSP48

USE_DSP48 Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	No
Spartan-3E	No
Virtex-II	No
Virtex-II Pro	No
Virtex-II Pro X	No
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner II	No

USE_DSP48 Applicable Elements

This constraint can be applied to an entire design via an XST command line, to a particular block (entity, architecture, component), and to a signal representing a macro described at the RTL level.

USE_DSP48 Description

USE_DSP48 is a synthesis constraint that allows control of Macro Implementation on Virtex-4. This constraint allows you to specify a technology resource (DSP48 or slices) that is used for macro implementation. The default value is "auto". In "auto" mode XST automatically implements such macros as MAC and accumulates on DSP48, but some of them as adders are implemented on slices. You have to force their implementation on DSP48 using a value of "yes" or "true". Please refer to the "HDL Coding Techniques" chapter of the XST User's Guide for supported macros and their implementation control.

Several macros (e.g., MAC), which can be placed on DSP48 are in fact a composition of more simple macros like multipliers, accumulators, and registers. In order to present the best performance, XST by default tries to infer and implement the maximum macro configuration. In a case you where you wish to shape a macro in a specific way, you have to use the KEEP constraint. For example, DSP48 allows you to implement a multiple with 2 input registers. In a case where you wish to leave the first register stage outside of DSP48, you have to place the KEEP constraint in their outputs.

Allowed values are AUTO, YES and NO (TRUE and FALSE are available in XCF as well). By default, safe implementation is enabled (AUTO).

USE_DSP48 Propagation Rules

Applies to an entity, component, module, or signal to which it is attached.

USE_DSP48 Syntax Examples

Schematic

Not applicable.

VHDL

Before using USE_DSP48, declare it with the following syntax:

```
attribute use_dsp48: string;
```

After USE_DSP48 has been declared, specify the VHDL constraint as follows:

```
attribute use_dsp48 of {entity_name|component_name|signal_name}:
{entity|component|signal} is "yes";
```

For a more detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute use_dsp48 [of] {module_name|signal_name} [is]
“yes”;
```

For a more detailed discussion of the basic Verilog syntax, see “Verilog”

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL “entity_name” use_dsp48={auto|yes|no|true|false};
BEGIN MODEL “entity_name”
  NET “signal_name” use_dsp48={auto|yes|no|true|false};
  END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **use_dsp48** command line option of the **run** command. Following is the basic syntax:

use_dsp48 {**AUTO**|**YES**|**NO**}

The default is **AUTO**.

Project Navigator

Set USE_DSP48 globally with the Use DSP48 option in the HDL Options tab of the Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

USE_RLOC

USE_RLOC Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

USE_RLOC Applicable Elements

Instances or macros that are members of sets.

USE_RLOC Description

USE_RLOC is an advanced mapping and placement constraint. It turns RLOC on or off for a specific element or section of a set. For more information about USE_RLOC, see "Toggling the Status of RLOC Constraints".

USE_RLOC Propagation Rules

It is illegal to attach USE_RLOC to a net. When attached to a design element, U_SET propagates to all applicable elements in the hierarchy within the design element.

USE_RLOC Syntax Examples

Schematic

Attach to a member of a set.

Attribute Name—USE_RLOC

Attribute Values—TRUE, FALSE

VHDL

Before using USE_RLOC, declare it with the following syntax:

```
attribute use_rloc: string;
```

After USE_RLOC has been declared, specify the VHDL constraint as follows:

```
attribute use_rloc of entity_name: entity is “true”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute use_rloc [of] module_name [is] “true”;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST “instance_name” USE_RLOC={TRUE|FALSE};
```

where

- **TRUE** turns on the RLOC constraint for a specific element.
- **FALSE** turns it off.

The default is **TRUE**.

XCF

```
MODEL “entity_name” use_rloc={true|false};
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

USE_SYNC_RESET

USE_SYNC_RESET Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner II	No

USE_SYNC_RESET Applicable Elements

This constraint can be applied to an entire design via an XST command line, to a particular block (entity, architecture, component), to a signal representing FF, and to an instance representing an instantiated FF.

USE_SYNC_RESET Description

USE_SYNC_RESET is a synthesis constraint that allows you (or prevents) a usage of a synchronous reset in the design. Detecting this constraint with a value of "no" or "false", XST avoids using synchronous reset resources in the final implementation. Moreover, for some designs, putting synchronous reset function on data input of the FF allows better logic optimization and therefore better QOR. In Auto mode XST tries to estimate a trade off between using dedicated Synchronous Reset input of an FF input and putting Synchronous Reset logic on D input of an FF. In a case where an FF is instantiated by the user, XST removes the synchronous reset only if the "Optimize Instantiated Primitives" switch is set to "yes".

Allowed values are AUTO, YES, and NO (TRUE and FALSE ones are available in XCF as well). By default, the usage of synchronous reset signal is enabled (AUTO).

USE_SYNC_RESET Propagation Rules

Applies to an entity, component, module, signal, or instance to which it is attached.

USE_SYNC_RESET Syntax Examples

Schematic

Not applicable.

VHDL

Before using USE_SYNC_RESET, declare it with the following syntax:

```
attribute use_sync_reset: string;
```

After USE_SYNC_RESET has been declared, specify the VHDL constraint as follows:

```
attribute use_sync_reset of
{entity_name|component_name|signal_name|instance_name}:
{entity|component|signal|label} is "no";
```

For a more detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute use_sync_reset [of]
{module_name|signal_name|instance_name} [is] no;
```

For a more detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL “entity_name” use_sync_reset={auto|yes|true|no|false};
BEGIN MODEL “entity_name”
  NET “signal_name” use_sync_reset={auto|yes|true|no|false};
  INST “instance_name” use_sync_reset={auto|yes|true|no|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-use_sync_reset** command line option of the **run** command. Following is the basic syntax:

```
-use_sync_reset {AUTO|YES|NO}
```

The default is **AUTO**.

Project Navigator

Set USE_SYNC_RESET globally with the Use Synchronous Reset option in the Xilinx Specific Options tab of the Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

USE_SYNC_SET

USE_SYNC_SET Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner II	No

USE_SYNC_SET Applicable Elements

This constraint can be applied to an entire design via an XST command line, to a particular block (entity, architecture, component), and to a signal representing an FF, and to an instance representing an instantiated FF.

USE_SYNC_SET Description

USE_SYNC_SET is a synthesis constraint that allows you (or prevents) a usage of a synchronous reset in the design. Detecting this constraint with a value of "no" or "false", XST avoids using synchronous reset resources in the final implementation. Moreover, for some designs, putting synchronous reset function on data input of the FF allows better logic optimization and therefore better QOR. In Auto mode XST tries to estimate a trade off between using dedicated Synchronous Set input of an FF input and putting Synchronous Set logic on D input of an FF. In a case where an FF is instantiated by the user, XST removes the synchronous reset only if the "Optimize Instantiated Primitives" switch is set to "yes".

Allowed values are AUTO, YES, and NO (TRUE and FALSE ones are available in XCF as well). By default, the usage of synchronous reset signal is enabled (AUTO).

USE_SYNC_SET Propagation Rules

Applies to an entity, component, module, signal, or instance to which it is attached.

USE_SYNC_SET Syntax Examples

Schematic

Not applicable.

VHDL

Before using USE_SYNC_SET, declare it with the following syntax:

```
attribute use_sync_set: string;
```

After USE_SYNC_SET has been declared, specify the VHDL constraint as follows:

```
attribute use_sync_set of
{entity_name|component_name|signal_name|instance_name}:
{entity|component|signal|label} is "no";
```

For a more detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute use_sync_set [of]
{module_name|signal_name|instance_name} [is] no;
```

For a more detailed discussion of the basic Verilog syntax, see “Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL “entity_name” use_sync_set={auto|yes|true|no|false};
BEGIN MODEL “entity_name”
  NET “signal_name” use_sync_set={auto|yes|true|no|false};
  INST “instance_name” use_sync_set={auto|yes|true|no|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-use_sync_set** command line option of the **run** command. Following is the basic syntax:

```
-use_sync_set {AUTO|YES|NO}
```

The default is **AUTO**.

Project Navigator

Set USE_SYNC_SET globally with the Use Synchronous Set option in the Xilinx Specific Options tab of the Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.

USELOWSKEWLINES

USELOWSKEWLINES Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	No
Spartan-3E	No
Virtex-II	No
Virtex-II Pro	No
Virtex-II Pro X	No
Virtex-4	No
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

USELOWSKEWLINES Applicable Elements

Nets

USELOWSKEWLINES Description

USELOWSKEWLINES is a PAR routing constraint.

Spartan-II, Spartan-IIE, Virtex and Virtex-E

The Spartan-II, Spartan-IIE, Virtex, and Virtex-E devices have 24 horizontal low skew resources which are intended to drive slower secondary clocks and may be used for high fanout nets. These 24 horizontal resources connect to the 12 vertical longlines in the column. The USELOWSKEWLINES constraint specifies the use of low skew routing resources for any net. You can use these resources for both internally generated and externally generated signals. Externally generated signals are those driven by IOBs.

USELOWSKEWLINES on a net directs PAR to route the net on one of the low skew resources. When this constraint is used, the timing tool automatically accounts for and reports skew on register-to-register paths that utilize those low skew resources.

Specify USELOWSKEWLINES only when all four primary global clocks have been used.

USELOWSKEWLINES Propagation Rules

Applies to attached net.

USELOWSKEWLINES Syntax Examples

Schematic

Attach to an output net.

Attribute Name—USELOWSKEWLINES

Attribute Values—TRUE, FALSE

VHDL

Before using USELOWSKEWLINES, declare it with the following syntax:

```
attribute uselowskewlines: string;
```

After USELOWSKEWLINES has been declared, specify the VHDL constraint as follows:

```
attribute uselowskewlines of signal_name : signal is “yes”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute uselowskewlines [of] signal_name [is] yes;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

This statement forces net $1I87/1N6745 to be routed on one of the device’s low skew resources.

```
NET “$1I87/$1N6745” USELOWSKEWLINES;
```

XCF

```
BEGIN MODEL “entity_name”
 NET “signal_name” uselowskewlines={yes|true};
END;
```

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

In the Misc tab, click Identify next to “Nets to use low Skew resources”. Complete the Low Skew Resource dialog box.

PCF

Same as the UCF syntax.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

VOLTAGE

VOLTAGE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

Availability depends on the release of characterization data.

VOLTAGE Applicable Elements

Global

VOLTAGE Description

VOLTAGE is an advanced timing constraint. It allows the specification of the operating voltage, which provides a means of prorating delay characteristics based on the specified voltage. Prorating is a scaling operation on existing speed file delays and is applied globally to all delays.

Each architecture has its own specific range of supported voltages. If the entered voltage does not fall within the supported range, the constraint is ignored and an architecture-specific default value is used instead. Also note that the error message for this condition appears during static timing.

VOLTAGE Propagation Rules

It is illegal to attach VOLTAGE to a net, signal, or design element.

VOLTAGE Syntax Examples

Schematic

Not applicable.

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

```
VOLTAGE=value [V];
```

where

- *value* is real number specifying the voltage
- V indicates volts, the default voltage unit

The following statement specifies that the analysis for everything relating to speed file delays assumes an operating power of 5 volts.

```
VOLTAGE=5;
```

XCF

Not applicable.

Constraints Editor

From the Project Navigator Processes window, access the Constraints Editor by double-clicking Create Timing Constraints under User Constraints.

In the Misc tab, click Specify next to “Voltage” and then fill out the Voltage dialog box.

PCF

The same as the UCF syntax.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

VREF

VREF Architecture Support

CoolRunner-II devices with 128 macrocells and larger.

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	No
Spartan-3E	No
Virtex-II	No
Virtex-II Pro	No
Virtex-II Pro X	No
Virtex-4	No
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	Yes*
* CoolRunner-II devices with 128 macrocells and larger.	

VREF Applicable Elements

Global.

VREF Description

VREF applies to the design as a global attribute (not directly applicable to any element in the design). The constraint configures listed pins as VREF supply pins to be used in conjunction with other I/O pins designated with one of the SSTL or HSTL I/O Standards.

Because VREF is selectable on any I/O in CoolRunner-II designs, this constraint allows you to select which pins will be VREF pins. Make sure you double-check pin assignment in

the report (RPT) file. If you do not specify any VREF pins for the differential I/O standards, HSTL and SSTL, or if you do not specify sufficient VREF pins within the required proximity of differential I/O pins, the fitter will automatically assign sufficient VREF.

VREF Propagation Rules

Configures listed pins as VREF supply pins to be used in conjunction with other I/O pins designated with one of the SSTL or HSTL I/O Standards.

VREF Syntax Examples

Schematic

VREF=*value_list* (on CONFIG symbol)

Legal values: P*nn* (where *nn* is a numeric pin number), *rc* (where *r*=alphabetic row, *c*=numeric column).

VHDL

Not applicable.

Verilog

Not applicable.

ABEL

Not applicable.

UCF/NCF

```
CONFIG VREF=value_list;
```

Legal values: P*nn* (where *nn* is a numeric pin number), *rc* (where r=alphabetic row, c=numeric column).

```
CONFIG VREF=P12,P13;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

WIREAND

WIREAND Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	No
Spartan-3E	No
Virtex-II	No
Virtex-II Pro	No
Virtex-II Pro X	No
Virtex-4	No
XC9500, XC9500XL, XC9500XV	Yes*
CoolRunner XPLA3	No
CoolRunner-II	No
* XC9500 only.	

WIREAND Applicable Elements

Any net.

WIREAND Description

WIREAND is an advanced fitter constraint. It forces a tagged node to be implemented as a wired AND function in the interconnect (UIM and Fastconnect).

WIREAND Propagation Rules

WIREAND is a net constraint. Any attachment to a design element is illegal.

WIREAND Syntax Examples

Schematic

Attach to a net.

Attribute Name—WIREAND

Attribute Values—TRUE, FALSE

VHDL

Before using WIREAND, declare it with the following syntax:

```
attribute wireand: string;
```

After WIREAND has been declared, specify the VHDL constraint as follows:

```
attribute wireand of signal_name : signal is “yes”;
```

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute wireand [of] signal_name [is] “yes”;
```

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

The following statement specifies that the net named SIG_11 be implemented as a wired AND when optimized.

```
NET “$I16789/SIG_11” WIREAND;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

WRITE_MODE

WRITE_MODE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

WRITE_MODE Applicable Elements

RAMB16_Sn

WRITE_MODE Description

WRITE_MODE is a basic mapping and a basic initialization constraint. It configures a single-port RAMB16 to support one of three write modes.

WRITE_MODE Propagation Rules

It is illegal to attach WRITE_MODE to a net.

When attached to a design element, WRITE_MODE propagates to all applicable elements in the hierarchy within the design element.

WRITE_MODE Syntax Examples

Schematic

Attach to a logic symbol.

Attribute Name—WRITE_MODE

Attribute Values—WRITE_FIRST, READ_FIRST, NO_CHANGE

VHDL

Before using WRITE_MODE, declare it with the following syntax:

```
attribute write_mode: string;
```

After WRITE_MODE has been declared, specify the VHDL constraint as follows:

```
attribute write_mode of {component_name|label_name}: {component|label}
is "{WRITE_FIRST|READ_FIRST|NO_CHANGE}";
```

See the UCF section for a description of WRITE_FIRST, READ_FIRST, and NO_CHANGE.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute write_mode [of] {module_name|instance_name}
[is] {WRITE_FIRST|READ_FIRST| NO_CHANGE};
```

See the UCF section for a description of WRITE_FIRST, READ_FIRST, and NO_CHANGE.

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name" WRITE_MODE={WRITE_FIRST|READ_FIRST|NO_CHANGE};
```

where

- WRITE_FIRST, the default, specifies that the location addressed is written before it is read. The new input data is written into the memory location and then transferred to the output register.
- READ_FIRST specifies that the location addressed is read before it is written. The current data in the memory location is transferred to the output register. The new data input is then written into the memory location.
- NO_CHANGE specifies that the output register retain the previous value. The new input data is written into the memory location. The output register value does not change.

The following statement sets the WRITE_MODE for the specified block RAMB16_Sn instance to READ_FIRST.

```
INST "$1I87/$1N6745" WRITE_MODE=READ_FIRST;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

WRITE_MODE_A

WRITE_MODE_A Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

WRITE_MODE_A Applicable Elements

Port A of RAMB16_Sm_Sn (dual-port block RAM)

WRITE_MODE_A Description

WRITE_MODE_A is a basic mapping and a basic initialization constraint. It configures port A (Sm) of a dual port RAMB16 to support one of three write modes.

WRITE_MODE_A Propagation Rules

It is illegal to attach WRITE_MODE_A to a net.

When attached to a design element, the constraint propagates to all applicable elements in the hierarchy within the design element.

WRITE_MODE_A Syntax Examples

Schematic

Attach to a logic symbol.

Attribute Name—WRITE_MODE_A

Attribute Values—WRITE_FIRST, READ_FIRST, NO_CHANGE

VHDL

Before using WRITE_MODE_A, declare it with the following syntax:

```
attribute write_mode_a: string;
```

After WRITE_MODE_A has been declared, specify the VHDL constraint as follows:

```
attribute write_mode_a of {component_name|entity_name|label_name}:
{compound|entity|label} is "{WRITE_FIRST|READ_FIRST|NO_CHANGE}";
```

See the UCF section for a description of WRITE_FIRST, READ_FIRST, and NO_CHANGE.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute write_mode_a [of] {module_name|instance_name}
[is] {WRITE_FIRST|READ_FIRST| NO_CHANGE};
```

See the UCF section for a description of WRITE_FIRST, READ_FIRST, and NO_CHANGE.

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST "instance_name" WRITE_MODE_A={WRITE_FIRST| READ_FIRST|NO_CHANGE};
```

where

- WRITE_FIRST, the default, specifies that the location addressed is written before it is read. The new input data is written into the memory location and then transferred to the output register.
- READ_FIRST specifies that the location addressed is read before it is written. The current data in the memory location is transferred to the output register. The new data input is then written into the memory location.
- NO_CHANGE specifies that the output register retain the previous value. The new input data is written into the memory location. The output register value does not change.

The following statement sets the write mode for port A of the specified block RAMB16_Sm_Sn instance to READ_FIRST.

```
INST "$1I87/$1N6745" WRITE_MODE_A=READ_FIRST;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

WRITE_MODE_B

WRITE_MODE_B Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	No
Virtex-E	No
Spartan-II	No
Spartan-IIE	No
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

WRITE_MODE_B Applicable Elements

Port B of RAMB16_Sm_Sn (dual-port block RAM)

WRITE_MODE_B Description

WRITE_MODE_B is a basic mapping and a basic initialization constraint. It configures port B (Sn) of a dual-port RAMB16 to support one of three write modes.

WRITE_MODE_B Propagation Rules

It is illegal to attach WRITE_MODE_B to a net. When attached to a design element, WRITE_MODE_B propagates to all applicable elements in the hierarchy within the design element.

WRITE_MODE_B Syntax Examples

Schematic

Attach to a logic symbol.

Attribute Name—WRITE_MODE_B

Attribute Values—WRITE_FIRST, READ_FIRST, NO_CHANGE

VHDL

Before using WRITE_MODE_B, declare it with the following syntax:

```
attribute write_mode_b: string;
```

After WRITE_MODE_B has been declared, specify the VHDL constraint as follows:

```
attribute write_mode_b of {compound_name|entity_name|label_name}:
{compound|entity|label} is “{WRITE_FIRST|READ_FIRST| NO_CHANGE}”;
```

See “WRITE_MODE_B Syntax Examples” for a description of WRITE_FIRST, READ_FIRST, and NO_CHANGE.

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
// synthesis attribute write_mode_b [of] {module_name|instance_name}
[is] {WRITE_FIRST|READ_FIRST|NO_CHANGE};
```

See “WRITE_MODE_B Syntax Examples” for a description of WRITE_FIRST, READ_FIRST, and NO_CHANGE.

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST “instance_name” WRITE_MODE_B={WRITE_FIRST|READ_FIRST|NO_CHANGE};
```

where

- WRITE_FIRST, the default, specifies that the location addressed is written before it is read. The new input data is written into the memory location and then transferred to the output register.
- READ_FIRST specifies that the location addressed is read before it is written. The current data in the memory location is transferred to the output register. The new data input is then written into the memory location.
- NO_CHANGE specifies that the output register retain the previous value. The new input data is written into the memory location. The output register value does not change.

The following statement sets the write mode for port B of the specified block RAMB16_Sm_Sn instance to READ_FIRST.

```
INST “$1I87/$1N6745” WRITE_MODE_B=READ_FIRST;
```

XCF

Not applicable.

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

XBLKNM

XBLKNM Architecture Support

Note: The numbers in the second column indicate applicable elements. See the next section, "XBLKNM Applicable Elements".

Architecture	Supported/Unsupported
Virtex	1, 2, 3, 4, 5, 6, 7
Virtex-E	1, 2, 3, 4, 5, 6, 7
Spartan-II	1, 2, 3, 4, 5, 6, 7
Spartan-IIE	1, 2, 3, 4, 5, 6, 7
Spartan-3	1, 2, 3, 5, 6, 7
Spartan-3E	1, 2, 3, 5, 6, 7
Virtex-II	1, 2, 3, 4, 5, 6, 7
Virtex-II Pro	1, 2, 3, 4, 5, 6, 7
Virtex-II Pro X	1, 2, 3, 4, 5, 6, 7
Virtex-4	1, 2, 3, 5, 6, 7
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

XBLKNM Applicable Elements

1. Flip-flop and latch primitives
2. Any I/O element or pad
3. FMAP
4. BUFT
5. ROM primitive
6. RAMS and RAMD primitives
7. Carry logic primitives

XBLKNM Description

XBLKNM is an advanced mapping constraint. It assigns block names to qualifying primitives and logic elements. If the same XBLKNM attribute is assigned to more than one

instance, the software attempts to pack logic with the same block name into one or more CLBs. Conversely, two symbols with different XBLKNM names are not mapped into the same block. Placing the same XBLKNMs on instances that do not fit within one block creates an error.

Specifying identical XBLKNM attributes on FMAP symbols tells the software to group the associated function generators into a single CLB. Using XBLKNM, you can partition a complete CLB without constraining the CLB to a physical location on the device.

Hierarchical paths are not prefixed to XBLKNM attributes, so XBLKNM attributes for different CLBs must be unique throughout the entire design.

The BLKNM attribute allows any elements except those with a different BLKNM to be mapped into the same physical component. XBLKNM, however, allows only elements with the same XBLKNM to be mapped into the same physical component. Elements without an XBLKNM cannot be not mapped into the same physical component as those with an XBLKNM.

XBLKNM Propagation Rules

Applies to the design element to which it is attached.

XBLKNM Syntax Examples

Schematic

Attach to a valid instance.

Attribute Name—XBLKNM

Attribute Values—*block_name*

where *block_name* is a valid block name for that type of symbol.

VHDL

Before using XBLKNM, declare it with the following syntax:

```
attribute xblknm: string;
```

After XBLKNM has been declared, specify the VHDL constraint as follows:

```
attribute xblknm of {component_name|label_name}: {component|label} is
"block_name";
```

where *block_name* is a valid block name for that type of symbol.

For a detailed discussion of the basic VHDL syntax, see "VHDL".

Verilog

Specify as follows:

```
 // synthesis attribute xblknm [of] {module_name|instance_name} [is]
block_name;
```

where *block_name* is a valid block name for that type of symbol.

For a detailed discussion of the basic Verilog syntax, see"Verilog".

ABEL

Not applicable.

UCF/NCF

The basic UCF syntax is:

```
INST “instance_name” XBLKNM=block_name;
```

where *block_name* is a valid block name for that type of symbol.

The following statement assigns an instantiation of an element named flip_flop2 to a block named U1358.

```
INST “$1I87/flip_flop2” XBLKNM=U1358;
```

XCF

```
BEGIN MODEL “entity_name”
 INST "instance_name" xblknm=xblknm_name;
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Not applicable.

Project Navigator

Not applicable.

XOR_COLLAPSE

XOR_COLLAPSE Architecture Support

The following table lists supported and unsupported architectures.

Architecture	Supported/Unsupported
Virtex	Yes
Virtex-E	Yes
Spartan-II	Yes
Spartan-IIE	Yes
Spartan-3	Yes
Spartan-3E	Yes
Virtex-II	Yes
Virtex-II Pro	Yes
Virtex-II Pro X	Yes
Virtex-4	Yes
XC9500, XC9500XL, XC9500XV	No
CoolRunner XPLA3	No
CoolRunner-II	No

XOR_COLLAPSE Applicable Elements

XOR_COLLAPSE applies to cascaded XORs.

XOR_COLLAPSE Description

XOR_COLLAPSE is synthesis constraint. It controls whether cascaded XORs should be collapsed into a single XOR. Allowed values are **yes** (check box is checked) and **no** (check box is not checked). (**TRUE** and **FALSE** ones are available in XCF as well). By default, XOR collapsing is enabled (**yes**).

XOR_COLLAPSE Propagation Rules

Not applicable

XOR_COLLAPSE Syntax Examples

Schematic

Not applicable.

VHDL

Before XOR_COLLAPSE can be used, it must be declared with the following syntax:

```
attribute xor_collapse: string;
```

After XOR_COLLAPSE has been declared, specify the VHDL constraint as follows:

```
attribute xor_collapse {signal_name|entity_name}: {signal|entity} is
“yes”;
```

The default value is **YES.**

For a detailed discussion of the basic VHDL syntax, see “VHDL”.

Verilog

Specify as follows:

```
 // synthesis attribute xor_collapse [of] {module_name|signal_name}
[is] yes;
```

The default value is **YES.**

For a detailed discussion of the basic Verilog syntax, see“Verilog”.

ABEL

Not applicable.

UCF/NCF

Not applicable.

XCF

```
MODEL “entity_name” xor_collapse={yes|no|true|false};

BEGIN MODEL “entity_name”
 NET “signal_name” xor_collapse={yes|no|true|false};
END;
```

Constraints Editor

Not applicable.

PCF

Not applicable.

Floorplanner

Not applicable.

PACE

Not applicable.

FPGA Editor

Not applicable.

XST Command Line

Define globally with the **-xor_collapse** command line option of the **run** command. Following is the basic syntax:

```
-xor_collapse {YES|NO}
```

The default is **YES**.

Project Navigator

Set globally with the XOR Collapsing option in the HDL Options tab of the Process Properties dialog box within the Project Navigator.

With a design selected in the Sources window, right-click Synthesize in the Processes window to access the appropriate Process Properties dialog box.