Young Jin Yoon

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Education

2008–2017 **Ph.D. in Computer Science**, *Columbia University*, New York, NY
Total GPA: *4.1414*/4.3
Advisor: Prof. Luca P. Carloni

2006–2007 **M.S. in Computer Science**, *Columbia University*, New York, NY
Total GPA: *3.8330*/4.3
Concentration: Network Systems

2000–2006 **B.S. in Computer Science and Engineering**, *Korea University*, Seoul, Korea
Total GPA: *3.99*/4.5 (*3.77*/4.0)
Major GPA: *4.24*/4.5 (*3.91*/4.0)

Work Experience

Vocational

2017- ***Software Engineer*** — *Intel Corporation*, Hillsboro, OR

Performance Engineering for Intel Omni-Path Architecture:
- Holistic performance analysis methodology for Omni-Path SW communication mechanisms.
- System bottleneck analysis for various high-performance applications.

2016 ***CAD Research Intern*** — *Intel Corporation*, Hillsboro, OR

Pre-silicon validation method to reuse post-silicon validation tools:
- A program to translate post-silicon validation commands into VP- and FPGA-specific commands
- Layered approach to the pre-silicon platform to avoid modification and reduce complexity

2012 ***Interim Engineering Intern*** — *Qualcomm NJ Research Center*, Bridgewater, NJ

High-level power and energy estimation tools for battery lifetime:
- Flexible and modular designs in C++ for future integration with simulators
- Hierarchical power estimation method with back-annotated power values

2011 ***Graduate Intern*** — *Intel Labs*, Hillsboro, OR

Synthesizable Intel On-chip System Fabric (IOSF) interface in SystemC:
- A generic Intel On-chip System Fabric (IOSF) interface in SystemC
- Parameterizable, flexible, and modular design for design space exploration

Academic

2008–2017 ***Research Assistant*** — *Columbia University*, New York, NY

Design space exploration and automation of Network-on-Chip (NoC) for future heterogeneous Systems-on-Chip:
- Integration of Communication Synthesis Infrastructure (COSI) and a time-approximate virtual platform for fast yet accurate NoC design space exploration
- Synthesizable and highly configurable NoC generation framework in SystemC
- Various RTL router design configuration and modification for the design space exploration
- An event-driven NoC simulator, and designed its plug-ins for full-system simulators to study the performance of chip-multiprocessors with various NoC configurations

2007–2010 ***Teaching Assistant*** — *Columbia University*, New York, NY

Teaching assistant for *CSEE4824: Computer Architecture*:
- Graded assignments, designed the class project, lectured some class sessions

Miscellaneous

2002–2004 ***Infantry Army Sergeant*** — *Republic of Korea Army*, Dongducheon, Korea

Korean Army Sergeant agreed to work at the 8^{th} U.S. Army in South Korea:
- Achievements: Warrior Leader Course Certification, Expert Infantryman Badge (EIB), and Physical Fitness Badge

Publications

2017 **Young Jin Yoon**, "Design and Optimization of Networks-on-Chip for Future Heterogeneous Systems-on-Chip", PhD thesis, Columbia University.

2013 **Young Jin Yoon**, Nicola Concer, Michele Petracca, and Luca Carloni, "Virtual Channels and Multiple Physical Networks: Two Alternatives to Improve NoC Performance", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems (TCAD)* 32.12, pp. 1906–1919.

2012 **Young Jin Yoon**, Nicola Concer, and Luca Carloni, "VENTTI: A Vertically Integrated Framework for Simulation and Optimization of Networks-on-Chip", in *IEEE International System-on-Chip Conference (SOCC)*, pp. 171–176.

2010 **Young Jin Yoon**, Nicola Concer, Michele Petracca, and Luca Carloni, "Virtual Channels vs. Multiple Physical Networks: a Comparative Analysis", in *Design Automation Conference (DAC)*, pp. 162–165.

2005 Jae-Ho Choi, **Young-Jin Yoon**, and Sangkeun Lee, "Efficient Dissemination of Filtered Data in XML-based Selective Dissemination of Information", in *Intl. Conf. on Database and Expert Systems Applications (DEXA)*, pp. 290–299.

Peer Review Activities

- ACM/IEEE Design Automation Conference (DAC) 2008–2010, 2016
- ACM/IEEE Design, Automation & Test in Europe Conf. (DATE) 2009, 2011–2015, 2017
- ACM/IEEE Intl. Symposium on Networks-on-Chip (NOCS) 2011–2016
- IEEE Symposium on High Performance Interconnects (HOTI) 2010, 2012–2013, 2015, 2016
- IEEE Transactions on Parallel and Distributed Systems (TPDS) 2014
- ACM Transactions on Architecture and Code Optimization (TACO) 2014
- Intl. Conference on Embedded Software (EMSOFT) 2009, 2014
- ACM-IEEE Intl. Conference on Formal Methods and Models for Codesign (MEMOCODE) 2013
- IFIP/IEEE Intl. Conference on Very Large Scale Integration (VLSI-SoC) 2013
- IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS) 2012
- IEEE Intl. Symposium on Industrial Embedded Systems (SIES) 2012
- The Intl. Conf. for High Perf. Comp., Networking, Storage and Analysis (SC) 2009–2010, 2012
- IEEE Intl. Symposium on High-Performance Computer Architecture (HPCA) 2011
- Intl. Green Computing Conference (IGCC) 2010
- Integration, the VLSI Jounal 2017
- IEEE/ACM Intl. Conference on Computer-Aided Design (ICCAD) 2008–2009

Technical skills

Computer Language

- *Software*: C/C++, JAVA, HTML/XML, Bash, Python
- *Hardware*: SystemC, Verilog/SystemVerilog, VHDL

IDEs & APIs

- Windows API, Visual C++, Eclipse, GIT,SVN, JSP, Xerces XML Parser

CAD Tools

- Synopsys Design Compiler/PrimeTime, Cadence CtoS compiler/Incisive/Virtuso

Natural Language

- English(*Fluent*), Korean(*Native*), Japanese(*Beginner*)

Selected Class Projects

2007 ***Revised Data Vortex Architecture*** *Optical Interconnect and Interconnection Networks*, Columbia University

Data Vortex architecture revision to provide a globally-fair arbitration mechanism:

- Proposed a revised Data Vortex architecture based on age-based arbitration.
- Provided both analytical and possible implementation details supported by simulations.

2007 ***Guitar Effects*** *Embedded System Design*, Columbia University

Various guitar effect implementations in VHDL and C:

- Designed guitar effects, such as distortion, vibrato, and chorus in VHDL and synthesized them on the *Altera* FPGA
- Implemented a control program in C running on a *NIOS* soft-core in the FPGA

2007 ***2.6Gb/s PC-Controlled Distributed Bit Error Rate Tester*** *Distributed Embedded System*, Columbia University

Distributed Bit Error Rate Tester (BERT) implementation in Verilog and Windows API:

- Designed two modules that can send and detect messages and errors up to 2.6 Gb/s in Verilog
- Implemented a program that can control 2 FPGAs and provide user interface with *Windows* API

2006–2007 ***THINC client in JAVA*** *Project in Computer Science*, Columbia University

Thin-client redesign and implementation in Java:

- Developed a thin-client based on "THINC: A Virtual Display Architecture for Thin-Client Computing"
- Implemented basic YV12, UYVY, and YUY2 pixel format converters in JAVA

Awards and Certifications

2012 ***Best in Session Award*** *SRC TECHCON 2012, Austin, TX*

2005, 2006 ***Scholarship*** *excellent GPA in fall 2004 and 2005, Korea University, Seoul, Korea*

2003 ***Graduation Certificate*** *Primary Leadership Development Course, the 8^{th} U.S. Army, Seoul, Korea*

1995 ***2nd Degree Black Belt in Taekwondo*** *Kukkiwon (Taekwondo HQ), Seoul, Korea*