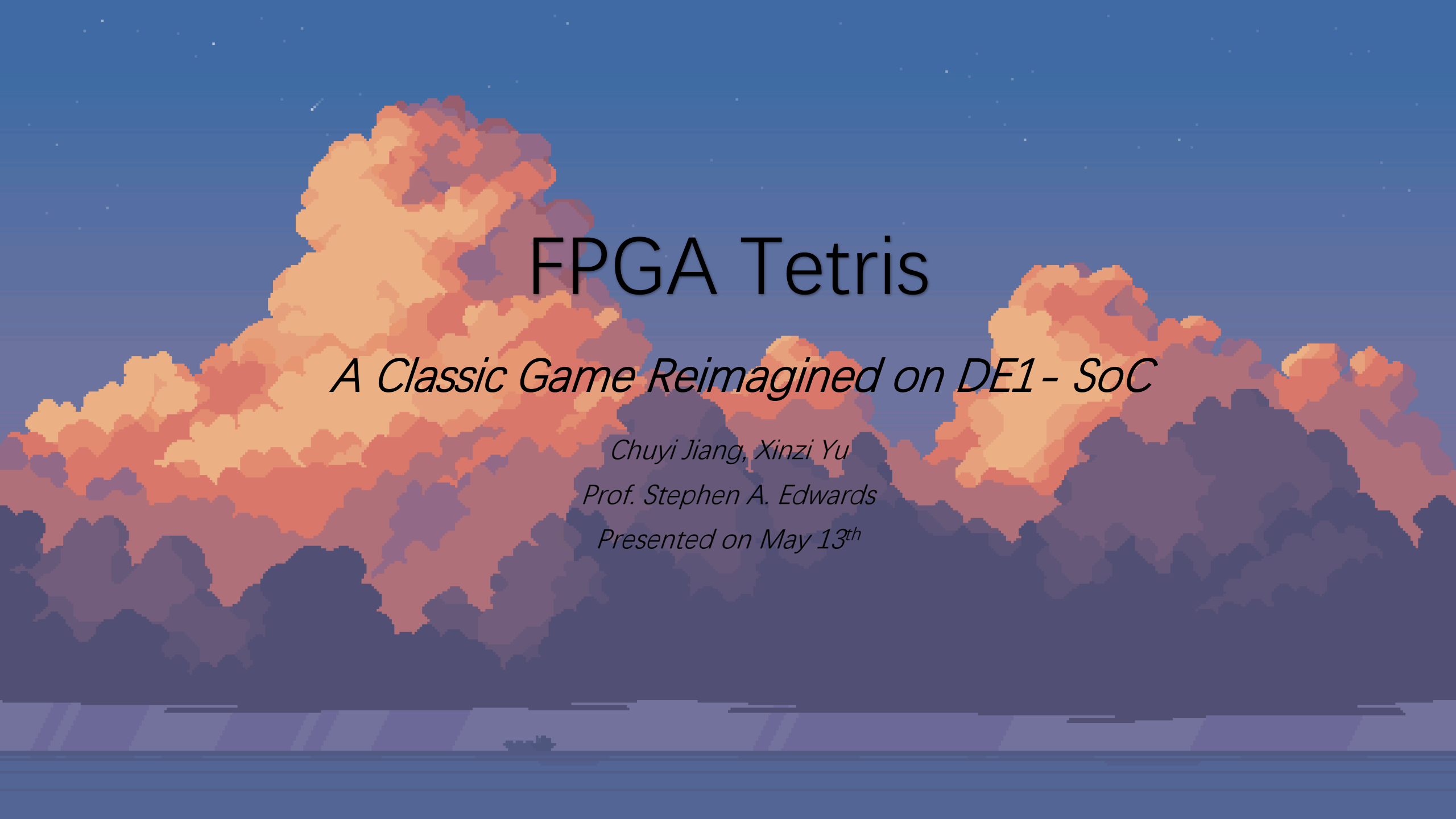


FPGA Tetris

A Classic Game Reimagined on DE1 - SoC

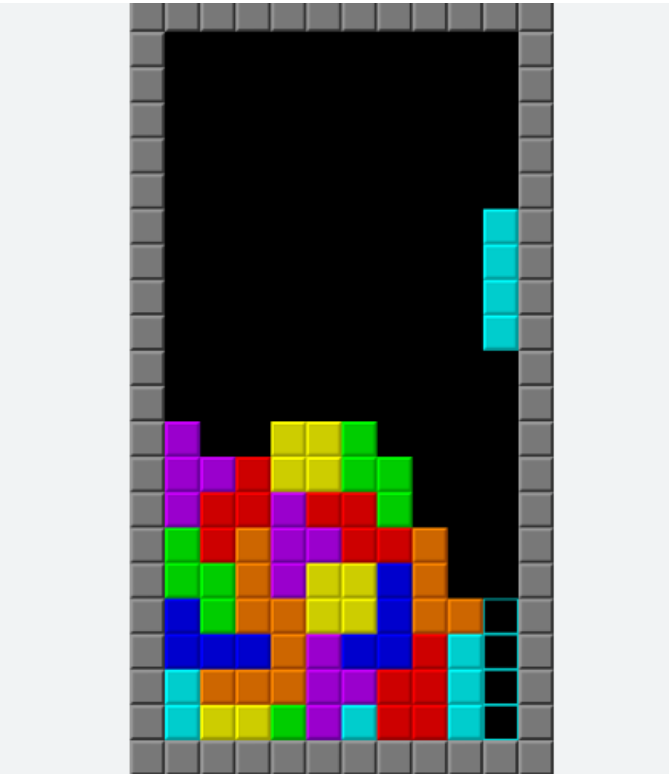
Chuyi Jiang, Xinzi Yu

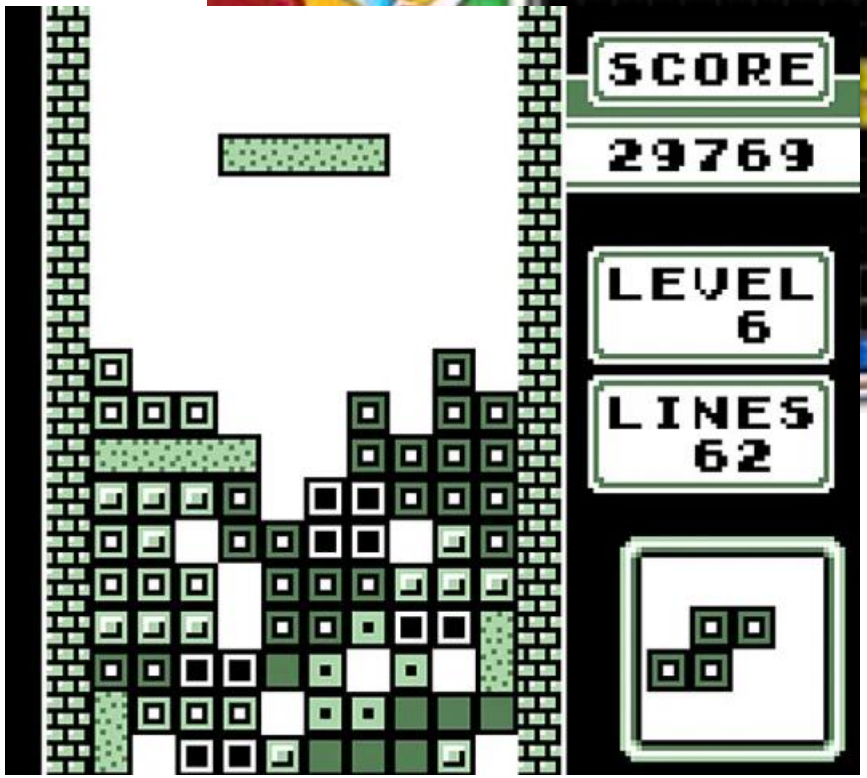
Prof. Stephen A. Edwards

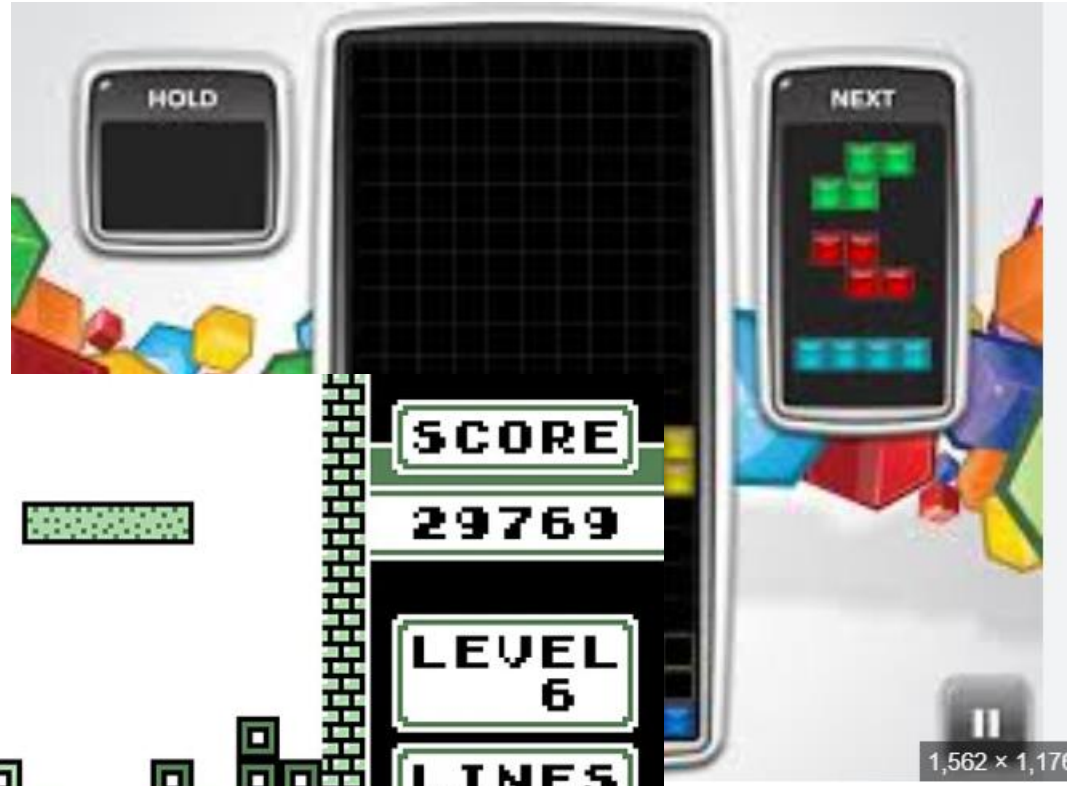
Presented on May 13th

What is Tetris?

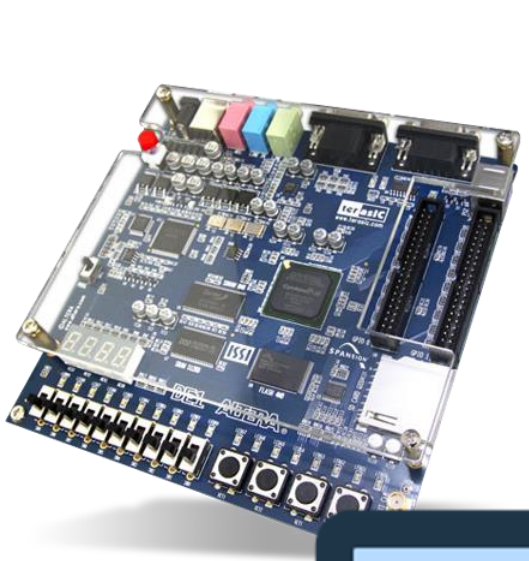
- A classic puzzle video game.

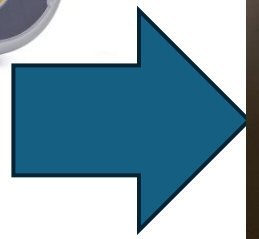


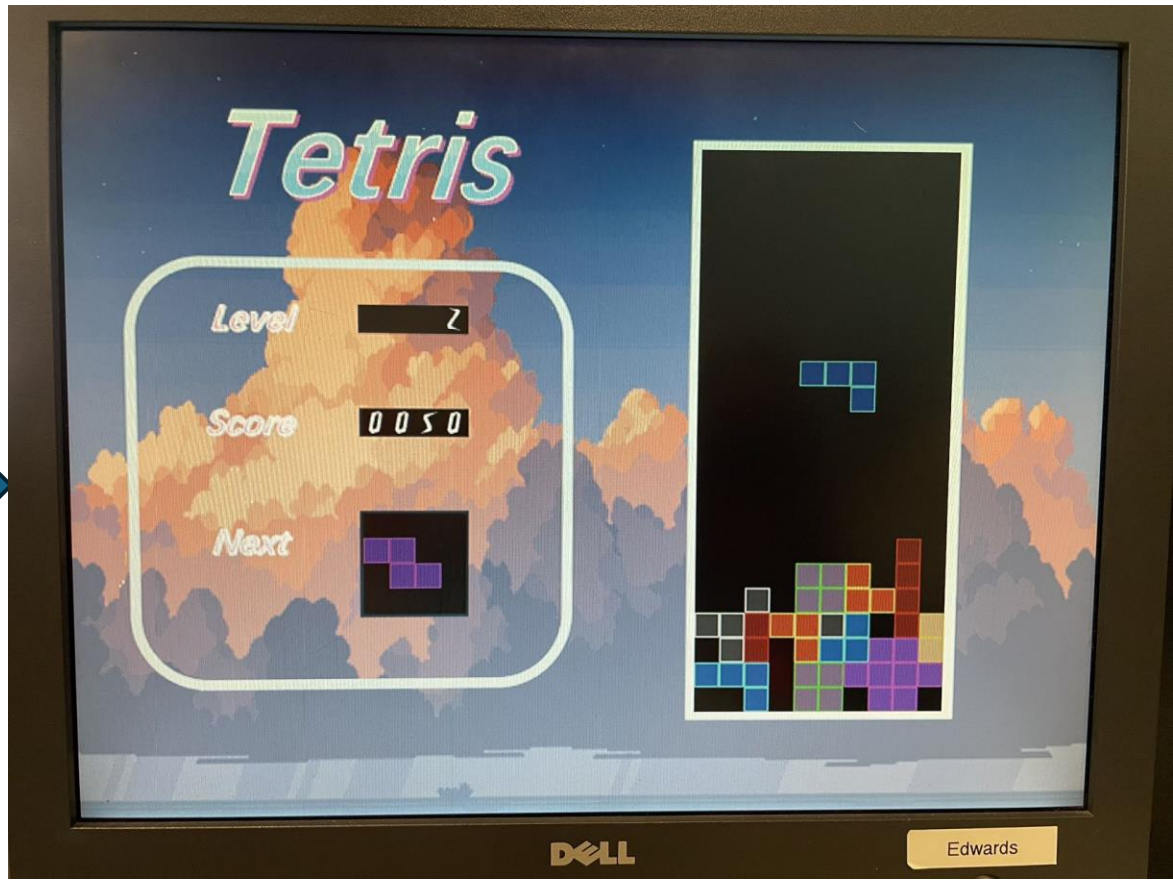




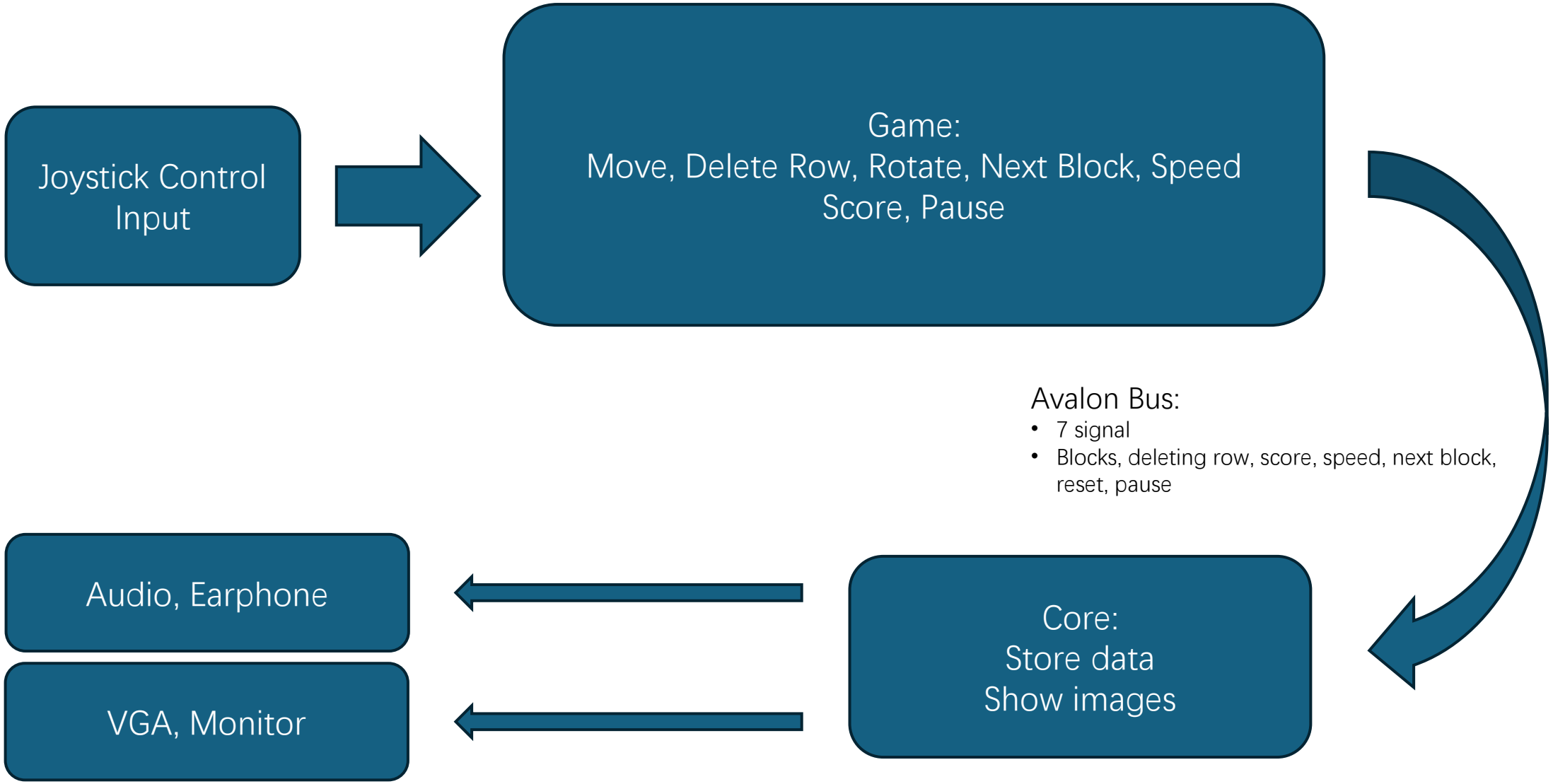
Overview







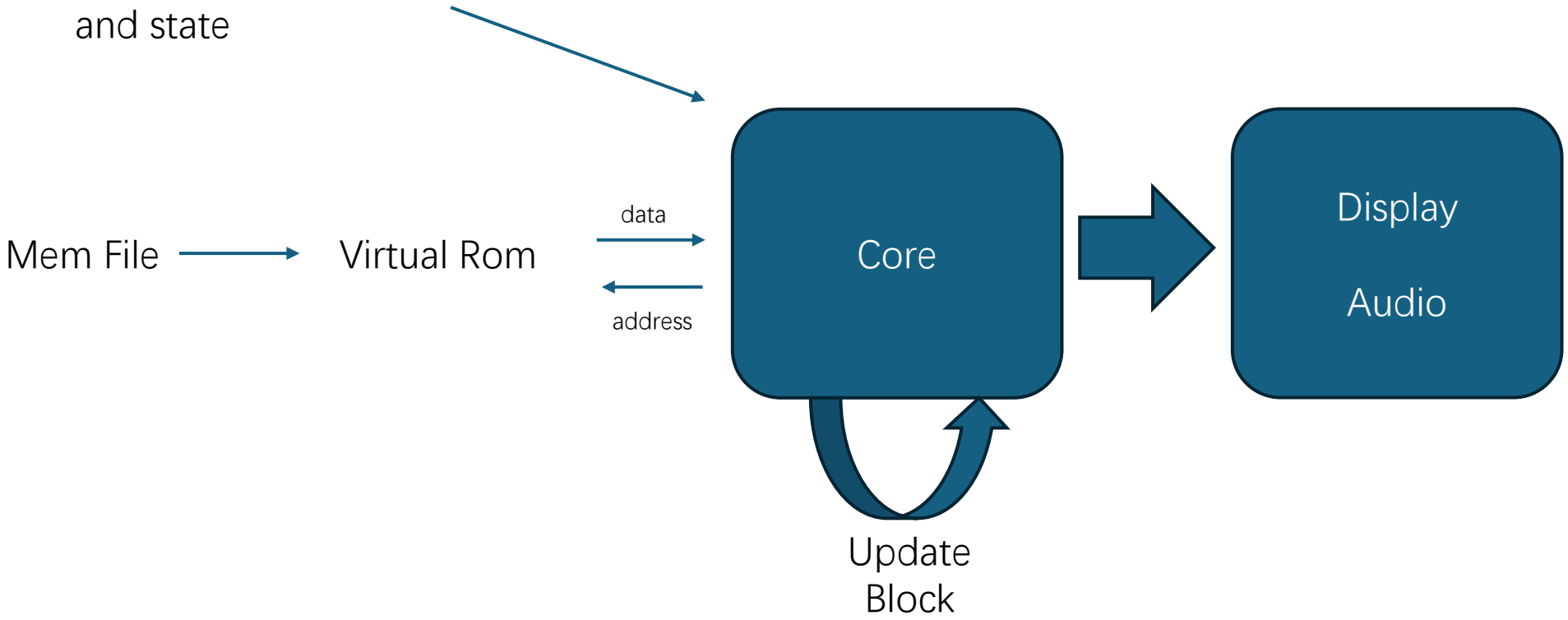
Architecture



Hardware Design

Avalon bus data:

- Give the information and state



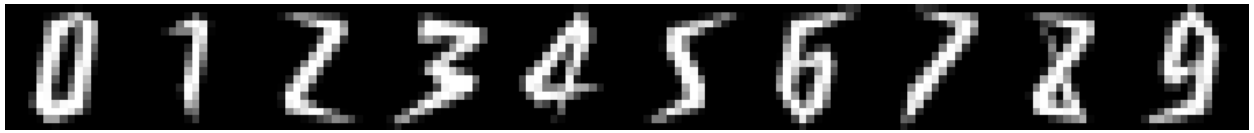
Graph

Color palette with 64 colors

Background

000110

000110

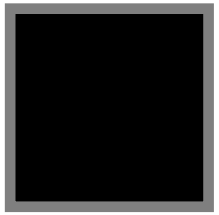


Score

640*512

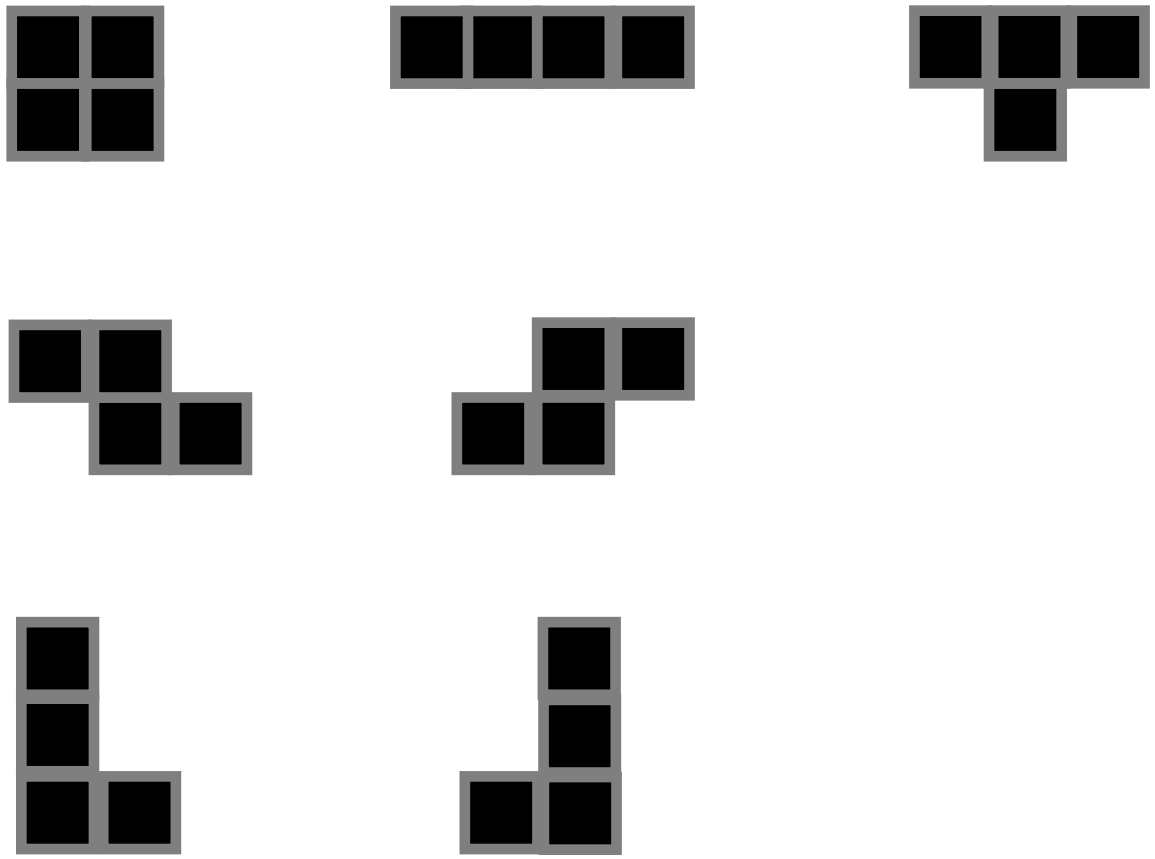
16*16

40*32

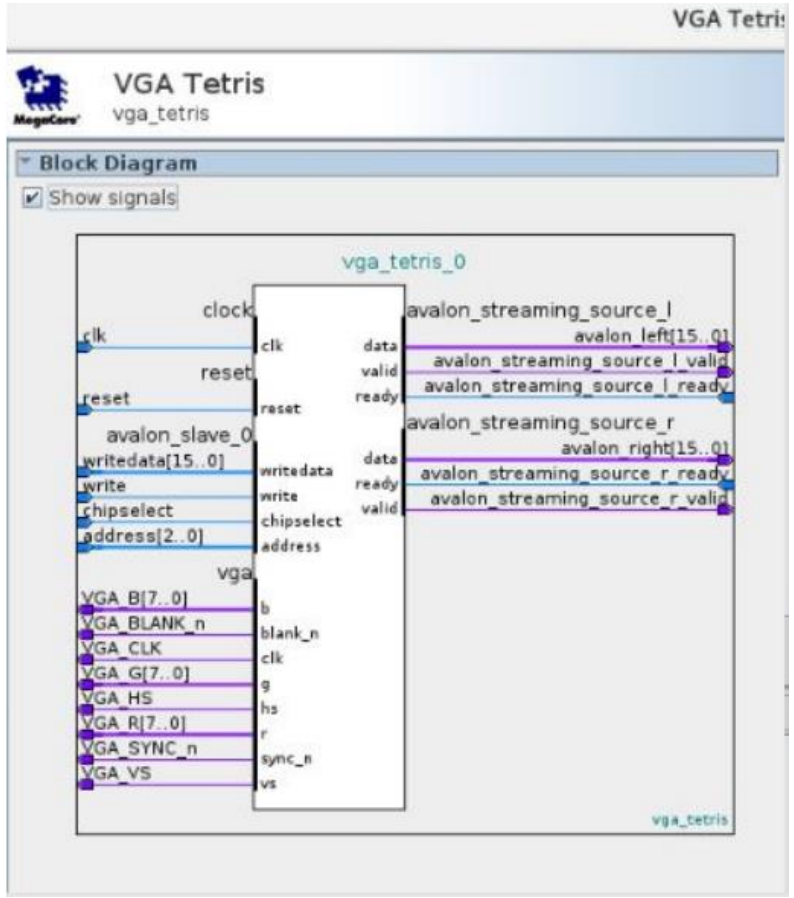


Block

Shape



Audio



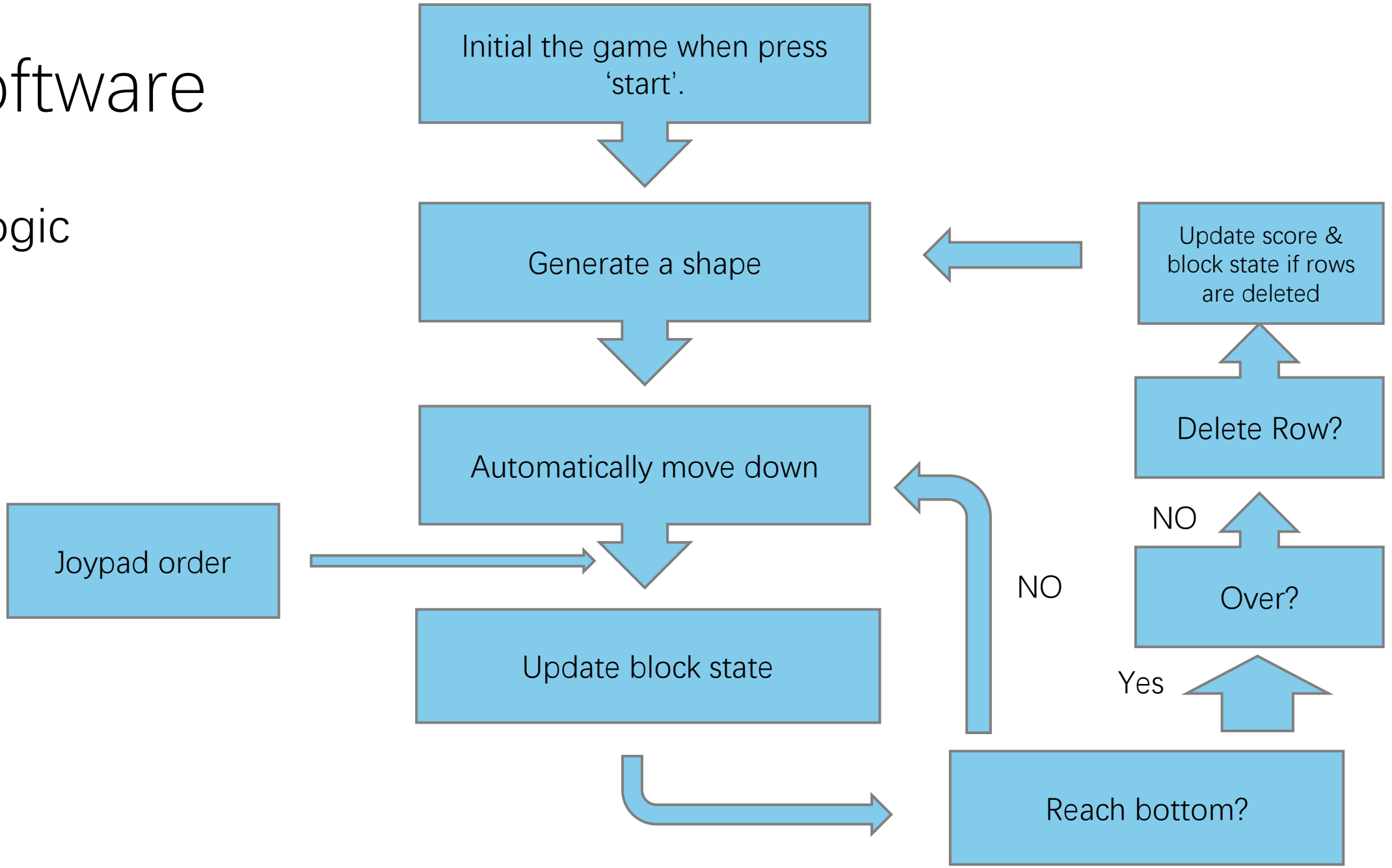
- 16 bits, 8kHz, mono Audio fragment
- Transfer .wav file to .mem
- The clock's frequency is 50MHz and our music's sample frequency is 8kHZ
- For different speed, use different constant to divide the clock frequency as equal to music's samples

Software

- Controller

Software

- Logic



Avalon Bus data

address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	row					column				type			rotation				Block information
1												num for deleted row					Row to delete
2	score 1					score 2				score 3			score 4				Scores
3														next type			Next Block type
4															speed		Speed
5															reset		Reset
6															o	p	Paused or Over

Conclusion

- Rom to store image and audio
- Joystick
- Further:
  - Add special audio when deleting rows
  - Create special tools help to quick deleting blocks when reaching certain scores
  - Support two players battling


Thank You!